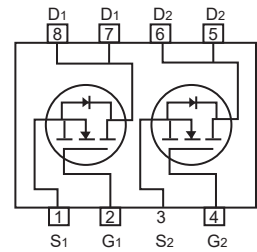
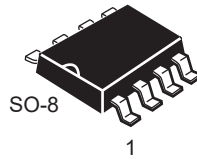


## Dual N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 100V, 3.1A,  $R_{DS(ON)} = 105m\Omega$  @ $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 140m\Omega$  @ $V_{GS} = 5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

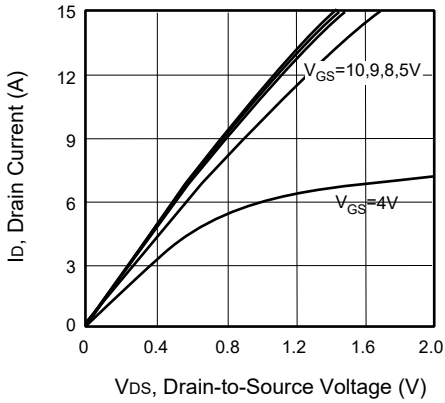
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	3.1	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	12.4	A
Maximum Power Dissipation	$P_D$	2	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

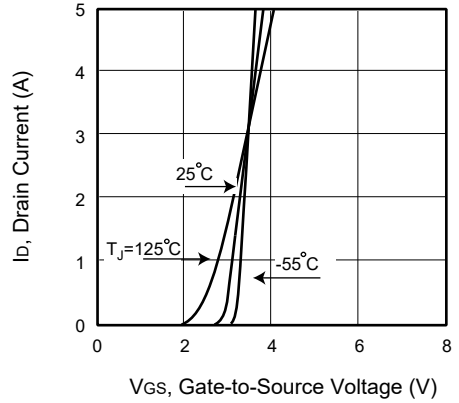
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

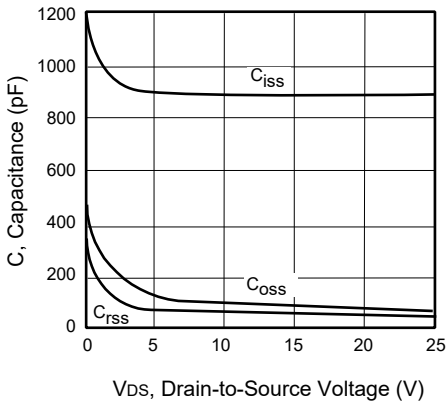
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1A$		80	105	$m\Omega$
		$V_{GS} = 5V, I_D = 1A$		98	140	$m\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		905		pF
Output Capacitance	$C_{oss}$			60		pF
Reverse Transfer Capacitance	$C_{rss}$			45		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 1A,$ $V_{GS} = 10V, R_{GEN} = 10\Omega$		15		ns
Turn-On Rise Time	$t_r$			4		ns
Turn-Off Delay Time	$t_{d(off)}$			37		ns
Turn-Off Fall Time	$t_f$			4		ns
Total Gate Charge	$Q_g$	$V_{DS} = 80V, I_D = 1A,$ $V_{GS} = 4.5V$		10		nC
Gate-Source Charge	$Q_{gs}$			2.2		nC
Gate-Drain Charge	$Q_{gd}$			5.4		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				1.6	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 1A$			1.2	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing.						



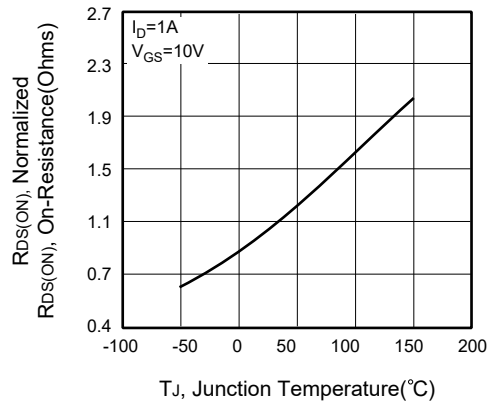
**Figure 1. Output Characteristics**



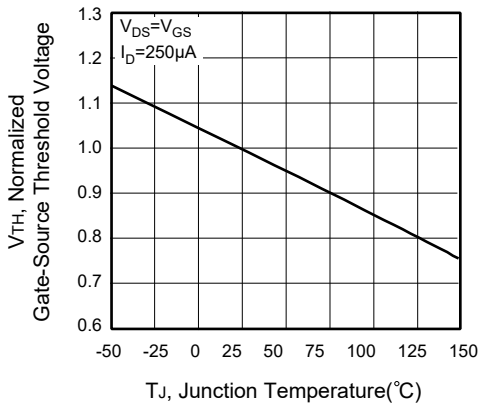
**Figure 2. Transfer Characteristics**



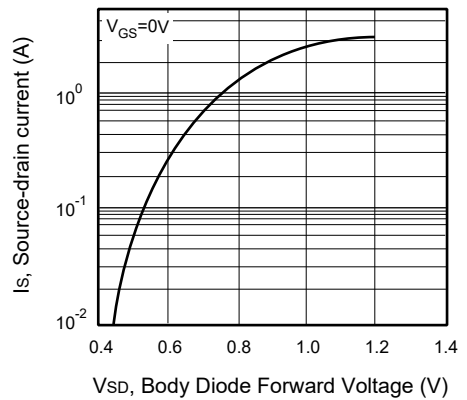
**Figure 3. Capacitance**



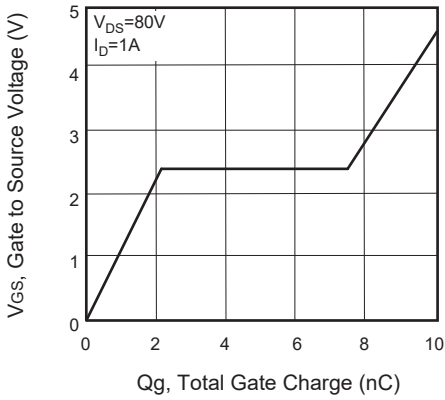
**Figure 4. On-Resistance Variation with Temperature**



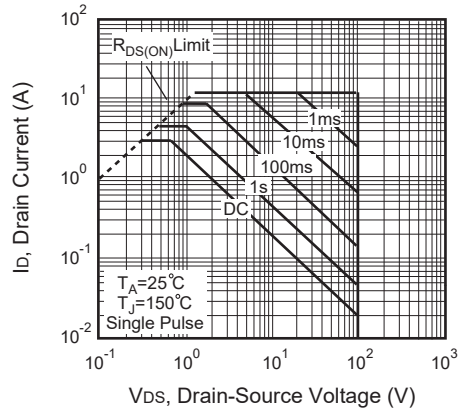
**Figure 5. Gate Threshold Variation with Temperature**



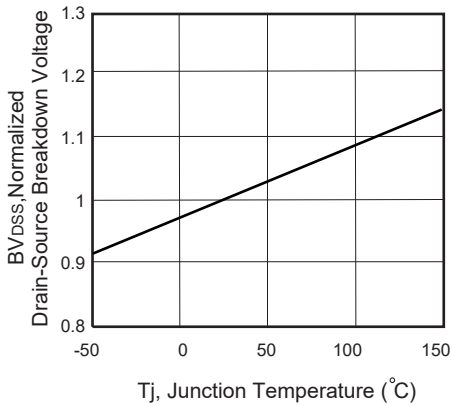
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



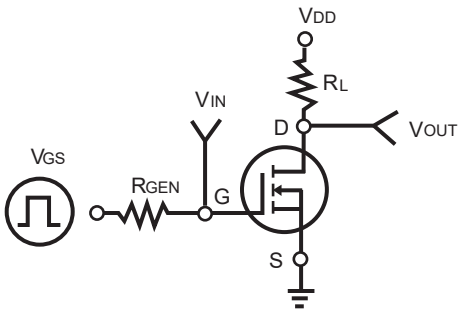
**Figure 7. Gate Charge**



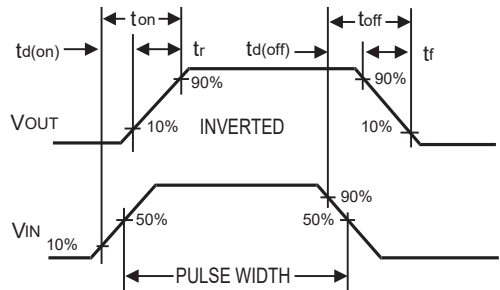
**Figure 8. Maximum Safe Operating Area**



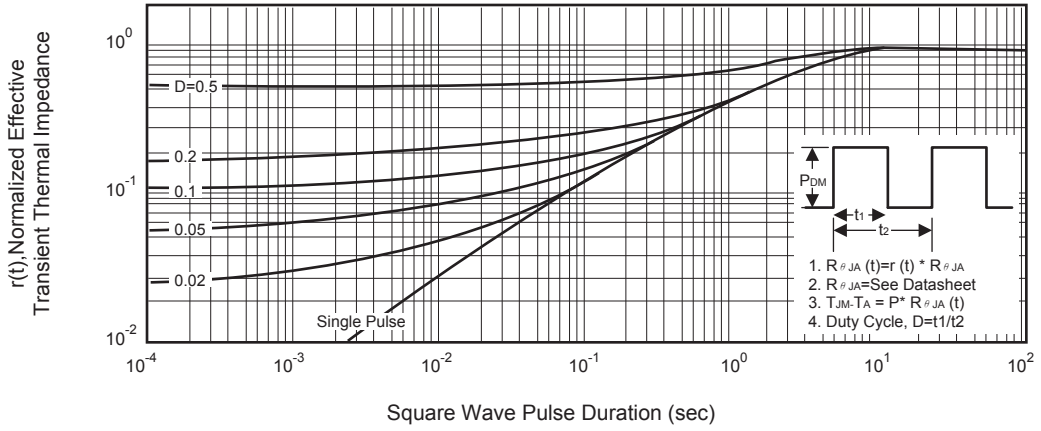
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**

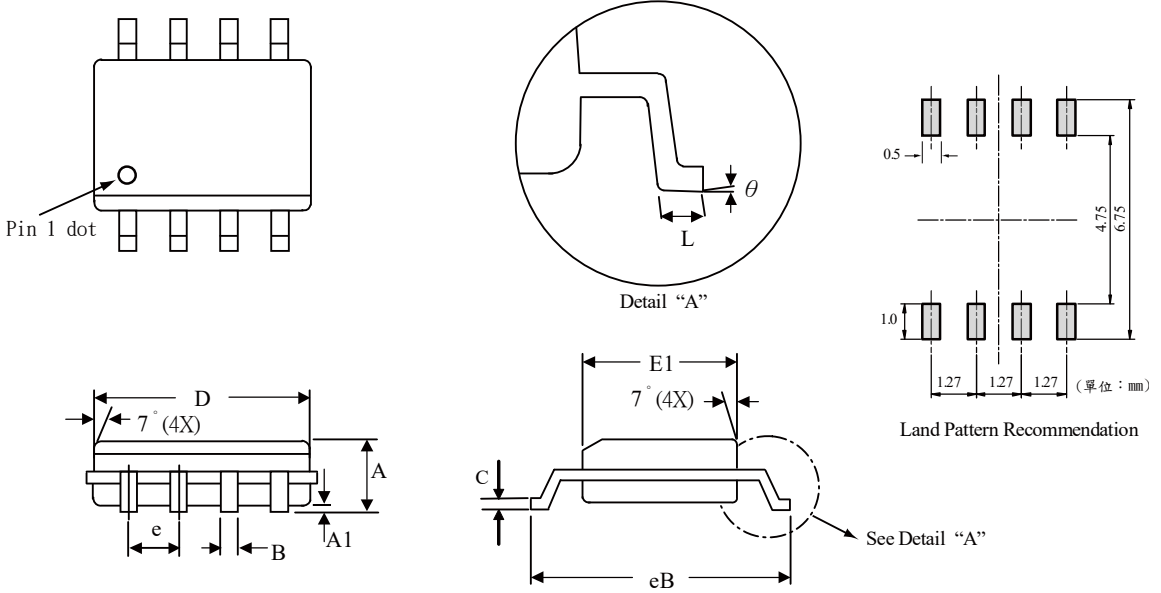


**Figure 11. Switching Waveforms**



**Figure 12. Normalized Thermal Transient Impedance Curve**

## SOP-8 產品外觀尺寸圖 (Product Outline Dimension)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.31	0.51	0.012	0.020
C	0.17	0.25	0.007	0.010
D	4.69	5.00	0.185	0.197
E1	3.70	4.06	0.146	0.160
eB	5.80	6.20	0.228	0.244
e	1.27		0.050	
L	0.40	0.95	0.016	0.037
$\theta$	0°	8°	0°	8°