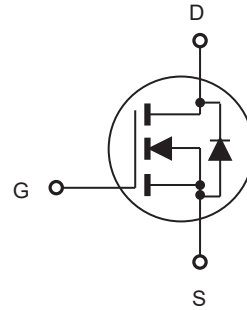
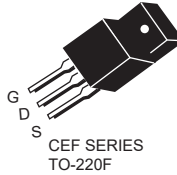


## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP11N65S	650V	0.42Ω	11A	10V
CEB11N65S	650V	0.42Ω	11A	10V
CEF11N65S	650V	0.42Ω	11A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	650		V
Gate-Source Voltage	V <sub>GS</sub>	±20		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	11	11 <sup>d</sup>	A
		7	7 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	44	44 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	125	31.2	W
		1	0.24	W/°C
Single Pulsed Avalanche Energy <sup>h</sup>	E <sub>AS</sub>	187		mJ
Single Pulsed Avalanche Current <sup>h</sup>	I <sub>AS</sub>	1.7		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1	4	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



# CEP11N65S/CEB11N65S CEF11N65S

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 5.5A$		0.35	0.42	$\Omega$
Gate Input Resistance	$R_g$	f=1MHz, open Drain		5.6		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		700		pF
Output Capacitance	$C_{oss}$			75		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 4.8A,$ $V_{GS} = 10V, R_{GEN} = 3.4\Omega$		23		ns
Turn-On Rise Time	$t_r$			9		ns
Turn-Off Delay Time	$t_{d(off)}$			46		ns
Turn-Off Fall Time	$t_f$			8		ns
Total Gate Charge	$Q_g$	$V_{DS} = 480V, I_D = 4.8A,$ $V_{GS} = 10V$		19		nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				11	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 5.5A^g$			1.2	V
Reverse Recovery Time	$T_{rr}$	$I_F = 5.5A,$ $di/dt = 100A/\mu s$		248		ns
Reverse Recovery Charge	$Q_{rr}$			1.9		$\mu C$
Peak Reverse Recovery Current	$I_{rr}$			13.4		A
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 5.5A$ . g.Full package $V_{SD}$ test condition $I_S = 5.5A$ . h.L = 130mH, $I_{AS} = 1.7A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25 \text{ C}$						



# CEP11N65S/CEB11N65S CEF11N65S

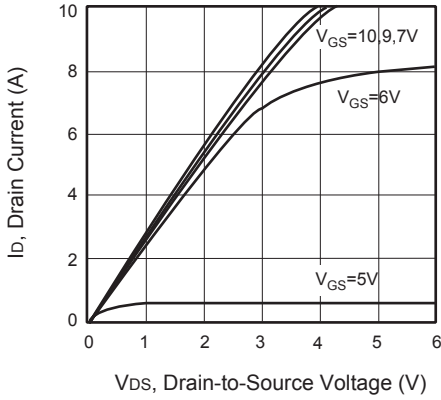


Figure 1. Output Characteristics

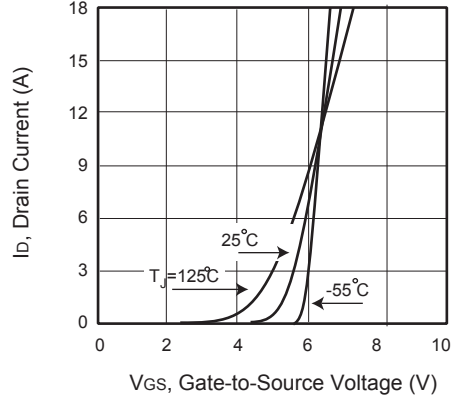


Figure 2. Transfer Characteristics

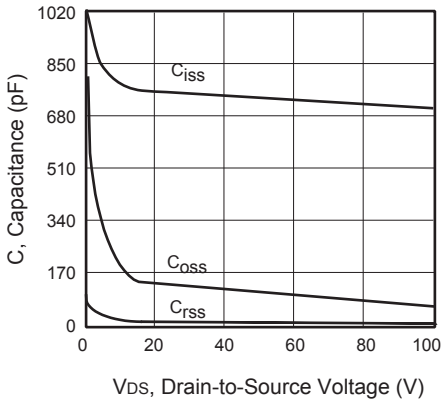


Figure 3. Capacitance

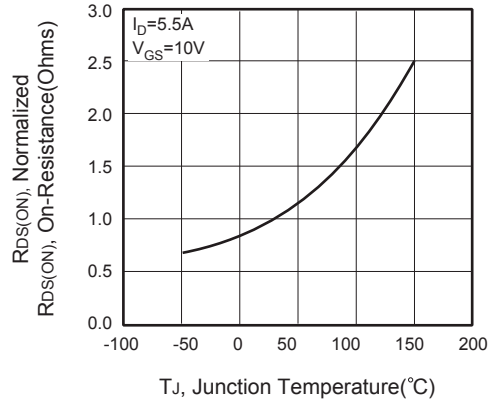


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

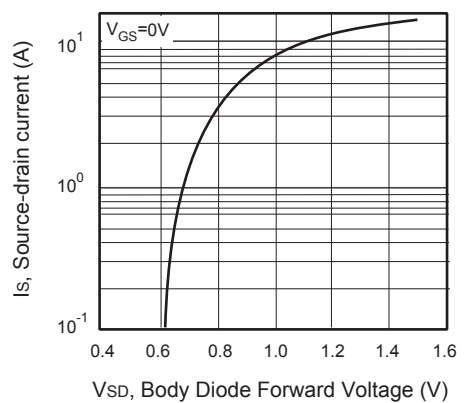


Figure 6. Body Diode Forward Voltage Variation with Source Current

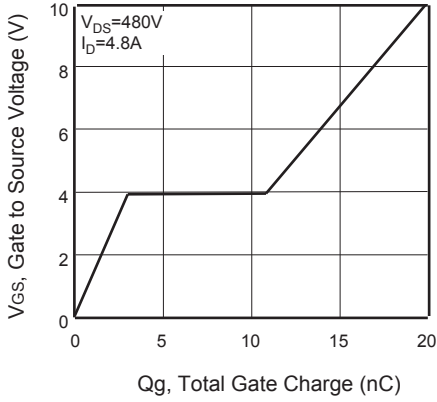


Figure 7. Gate Charge

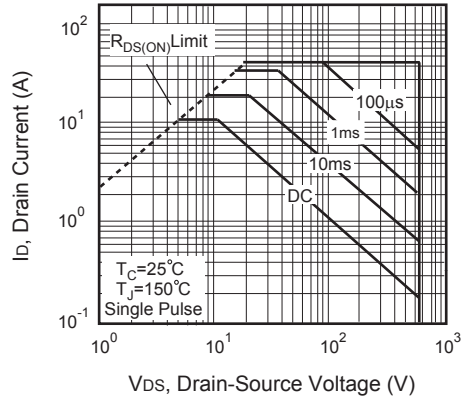


Figure 8. Maximum Safe Operating Area

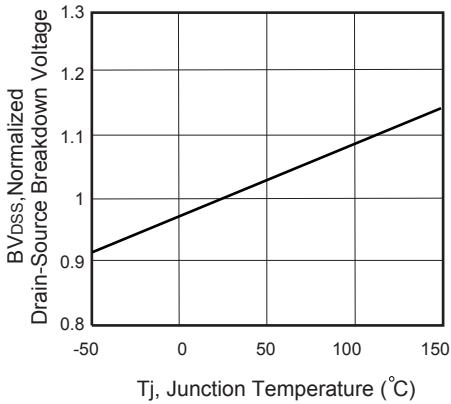


Figure 9. Breakdown Voltage Variation VS Temperature

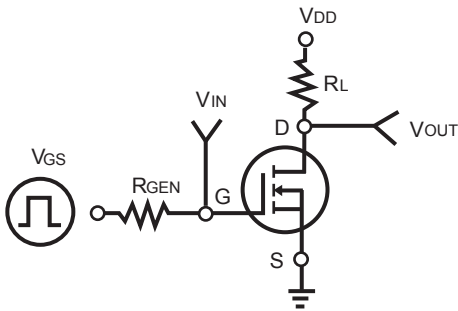


Figure 10. Switching Test Circuit

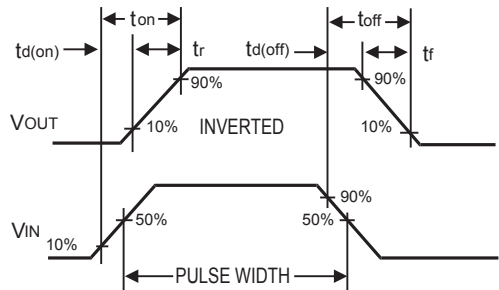


Figure 11. Switching Waveforms



# CEP11N65S/CEB11N65S CEF11N65S

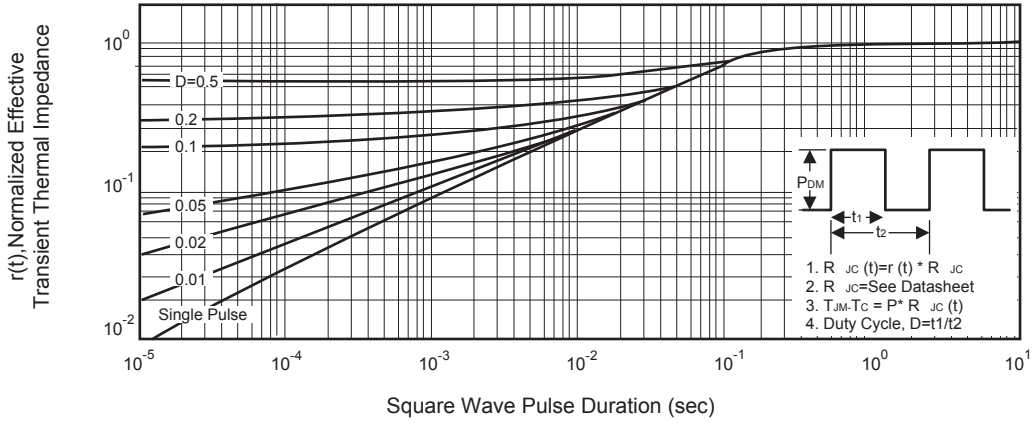


Figure 12. Normalized Thermal Transient Impedance Curve