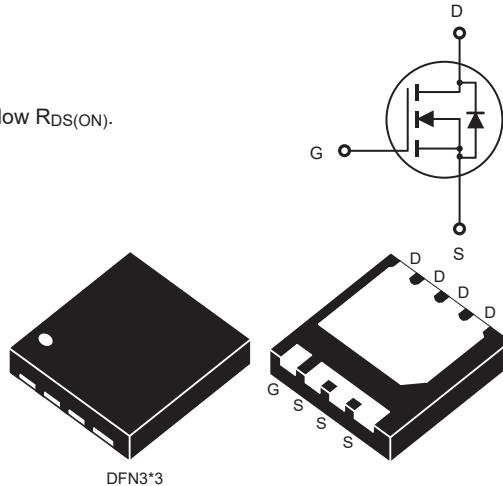


## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 40V, 40A,  $R_{DS(ON)} = 10.2 \text{ m}\Omega$  @ $V_{GS} = 10\text{V}$ .  
 $R_{DS(ON)} = 16 \text{ m}\Omega$  @ $V_{GS} = 4.5\text{V}$ .
- Super High dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS

$T_C = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	40	A
	$I_D @ R_{\theta JA}$	12	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{\theta JC}$	160	A
	$I_{DM} @ R_{\theta JA}$	48	A
Maximum Power Dissipation	$P_D$	25	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

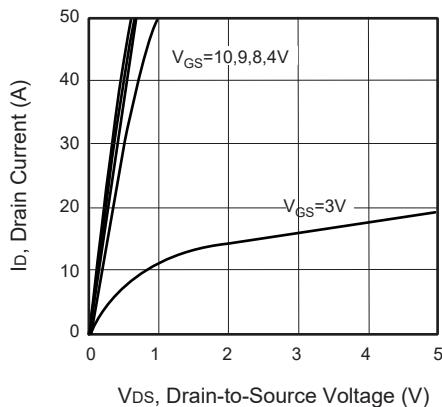
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case <sup>b</sup>	$R_{\theta JC}$	5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	50	$^\circ\text{C/W}$



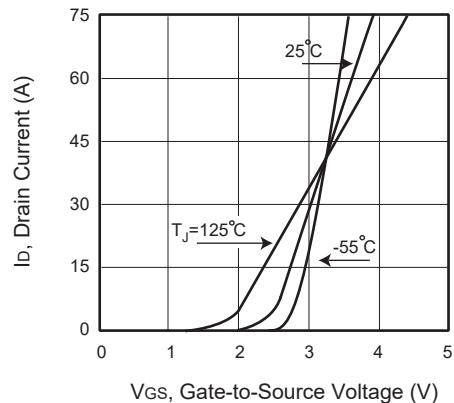
# CEC4112A

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

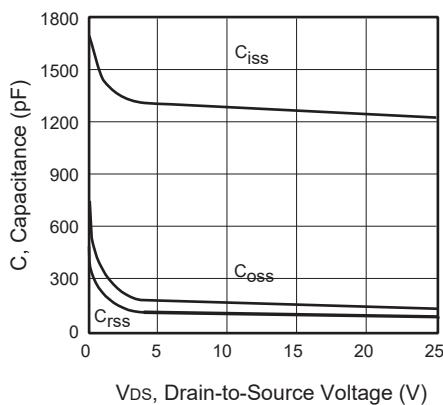
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$			1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	1		3	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_D = 10\text{A}$		8.2	10.2	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 8\text{A}$		10	16	$\text{m}\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		1220		pF
Output Capacitance	$C_{\text{oss}}$			150		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			115		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 32\text{V}, I_D = 10\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		22		ns
Turn-On Rise Time	$t_r$			13		ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			61		ns
Turn-Off Fall Time	$t_f$			13		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 32\text{V}, I_D = 10\text{A}, V_{\text{GS}} = 4.5\text{V}$		14.6		nC
Gate-Source Charge	$Q_{\text{gs}}$			2.5		nC
Gate-Drain Charge	$Q_{\text{gd}}$			9.7		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				20	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 15\text{A}$			1.2	V
<b>Notes :</b>						
a.Repetitive Rating : Pulse width limited by maximum junction temperature						
b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 2\%$ .						
c.Guaranteed by design, not subject to production testing.						



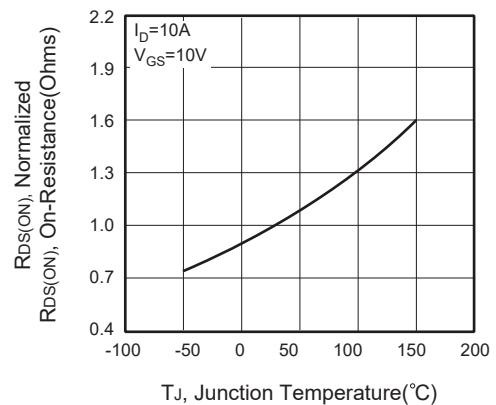
**Figure 1. Output Characteristics**



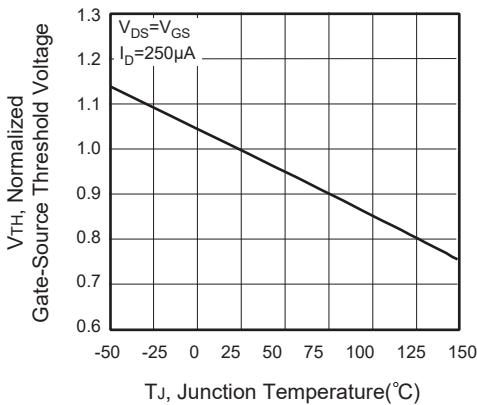
**Figure 2. Transfer Characteristics**



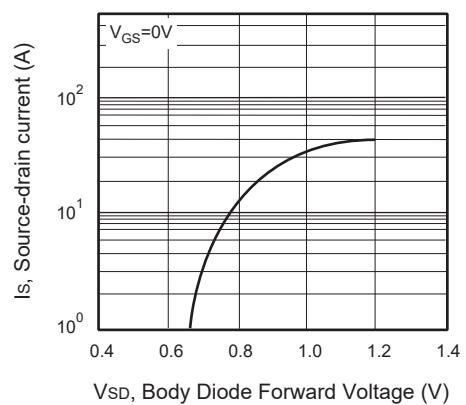
**Figure 3. Capacitance**



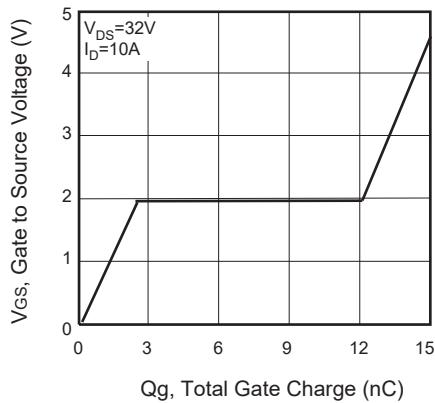
**Figure 4. On-Resistance Variation with Temperature**



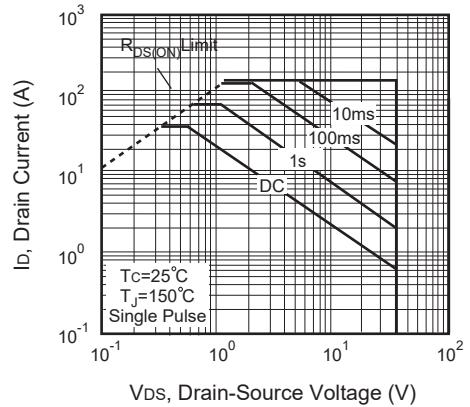
**Figure 5. Gate Threshold Variation with Temperature**



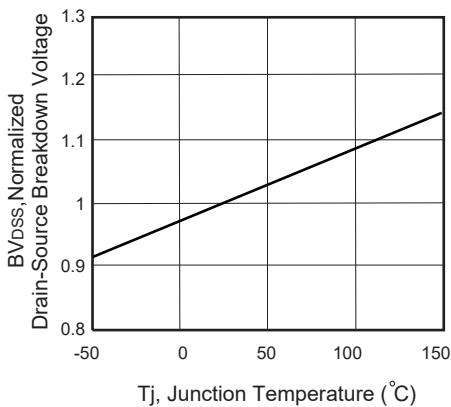
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



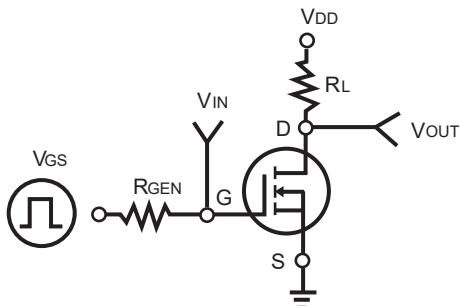
**Figure 7. Gate Charge**



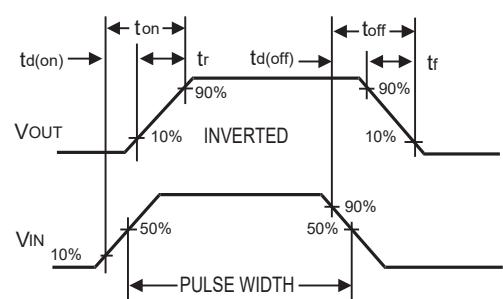
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**

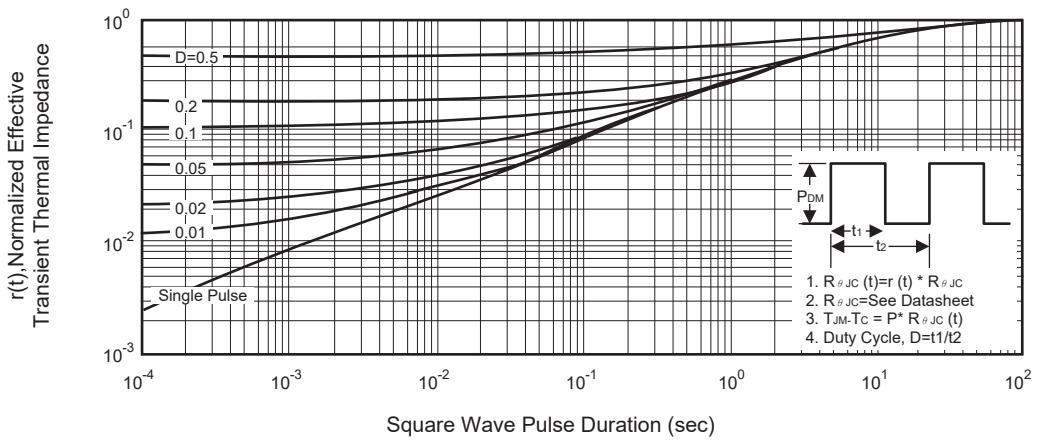


Figure 12. Normalized Thermal Transient Impedance Curve