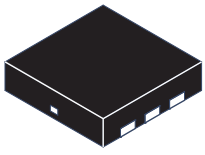
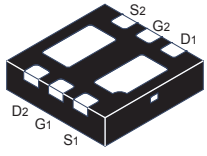
CEC2609

Dual Enhancement Mode Field Effect Transistor (N and P Channel) PRELIMINARY

FEATURES

- 20V, 4.8A, $R_{DS(ON)}$ = 38mΩ @V_{GS} = 4.5V.
  $R_{DS(ON)}$ = 55mΩ @V_{GS} = 2.5V.
- -20V, -3.0A, $R_{DS(ON)}$ = 100mΩ @V_{GS} = -4.5V.
  $R_{DS(ON)}$ = 145mΩ @V_{GS} = -2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.





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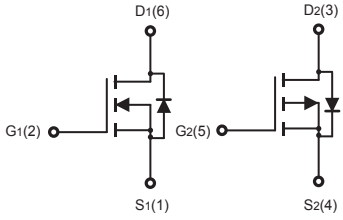

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±12	±12	V
Drain Current-Continuous	I_D@T_A = 25°C	4.8	-3.0	A
	I_D@T_A = 70°C	3.8	-2.3	A
Drain Current-Pulsed [a]	I_{DM}	19.2	-12	A
Maximum Power Dissipation	P_D	1.31		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case [b]	$R_{\theta Jc}$	30	°C/W
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	95	°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	0.4		1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3.5A		29	38	mΩ
		V_{GS} = 2.5V, I_D = 2.0A		37	55	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f = 1.0 MHz		380		pF
Output Capacitance	C_{oss}			90		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 3.5A, V_{GS} = 4.5V, R_{GEN} = 6Ω		16		ns
Turn-On Rise Time	t_r			16		ns
Turn-Off Delay Time	$t_{d(off)}$			32		ns
Turn-Off Fall Time	t_f			7		ns
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 3.5A, V_{GS} = 3.3V		3.6		nC
Gate-Source Charge	Q_{gs}			1.0		nC
Gate-Drain Charge	Q_{gd}			1.2		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1A			1.1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-CHANNEL Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-0.4		-1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.5A		78	100	mΩ
		V_{GS} = -2.5V, I_D = -1.5A		110	145	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -10V, V_{GS} = 0V, f = 1.0 MHz		375		pF
Output Capacitance	C_{oss}			90		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10V, I_D = -2.5A, V_{GS} = -4.5V, R_{GEN} = 3Ω		17		ns
Turn-On Rise Time	t_r			17		ns
Turn-Off Delay Time	$t_{d(off)}$			27		ns
Turn-Off Fall Time	t_f			7		ns
Total Gate Charge	Q_g	V_{DS} = -10V, I_D = -2.0A, V_{GS} = -3.3V		2.9		nC
Gate-Source Charge	Q_{gs}			0.46		nC
Gate-Drain Charge	Q_{gd}			1.19		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-1	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t < 5 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

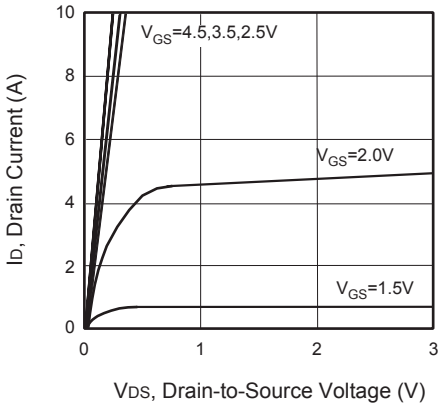

Figure 1. Output Characteristics

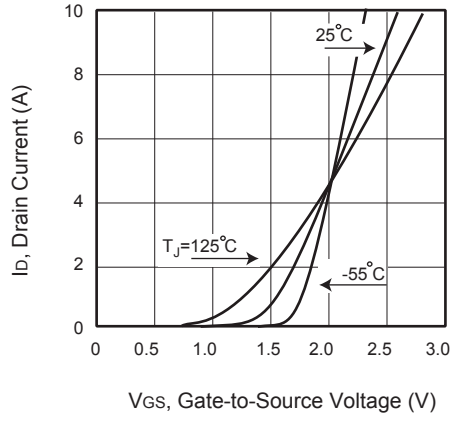

Figure 2. Transfer Characteristics

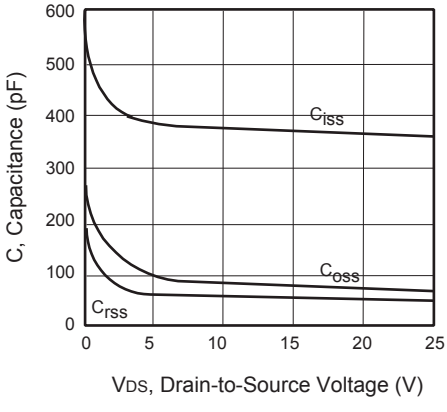

Figure 3. Capacitance

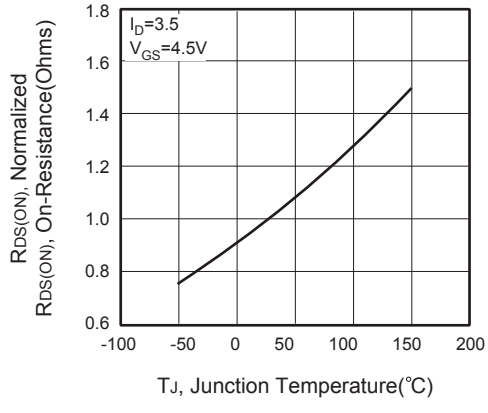

Figure 4. On-Resistance Variation with Temperature

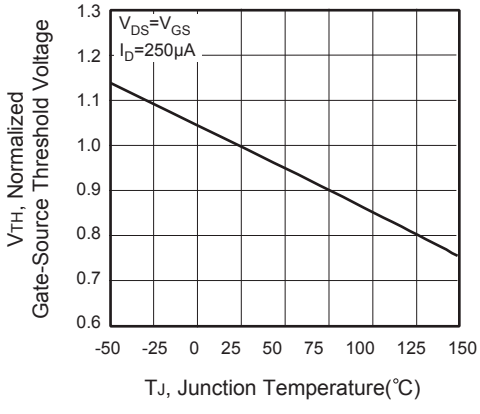

Figure 5. Gate Threshold Variation with Temperature

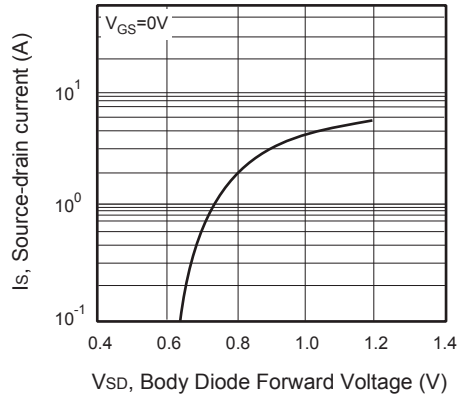

Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

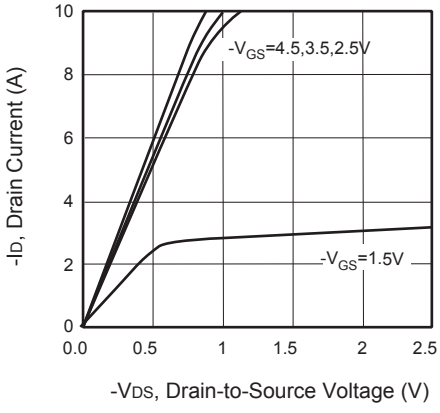

Figure 7. Output Characteristics

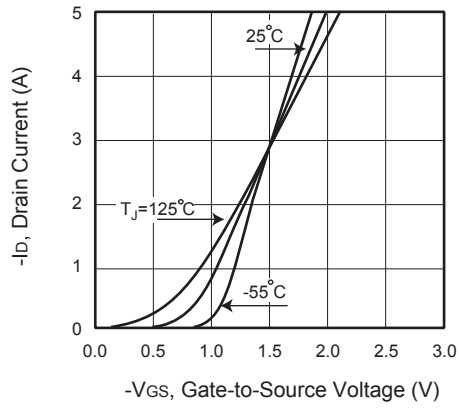

Figure 8. Transfer Characteristics

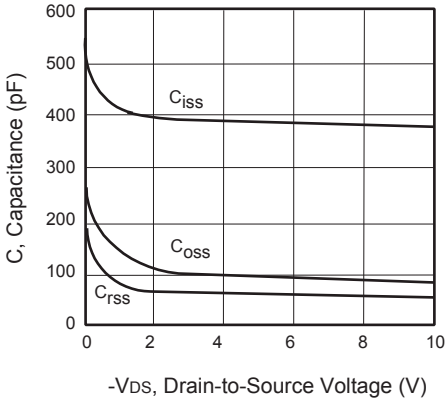

Figure 9. Capacitance

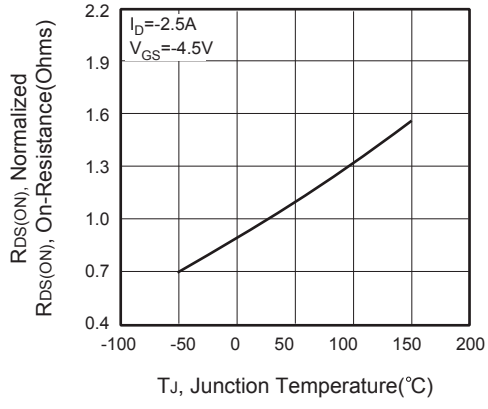

Figure 10. On-Resistance Variation with Temperature

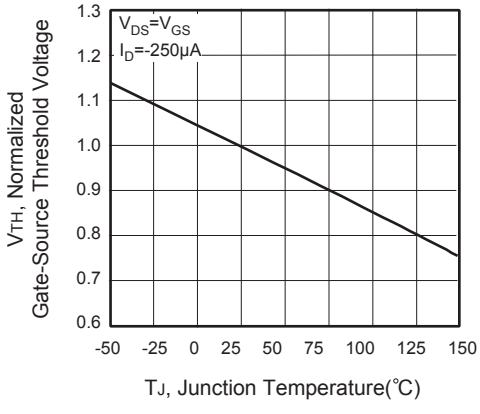

Figure 11. Gate Threshold Variation with Temperature

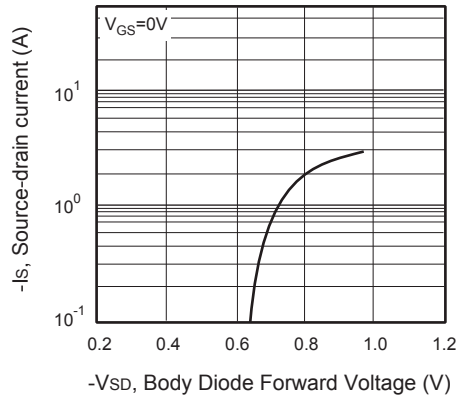

Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

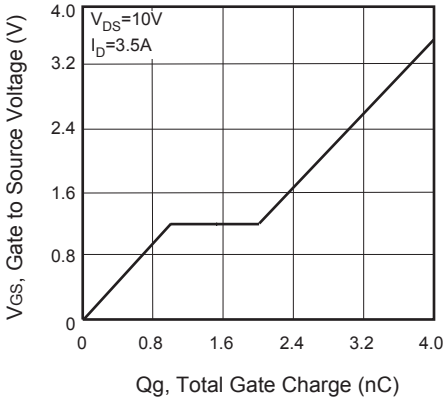

Figure 13. Gate Charge

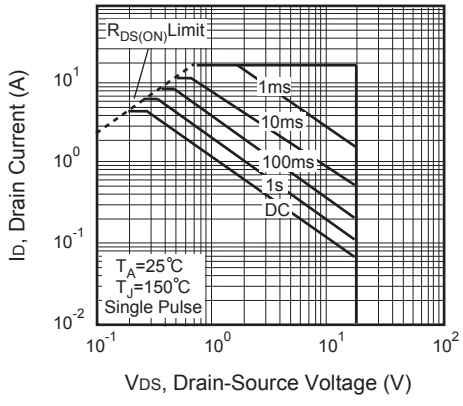

Figure 14. Maximum Safe Operating Area

P-CHANNEL

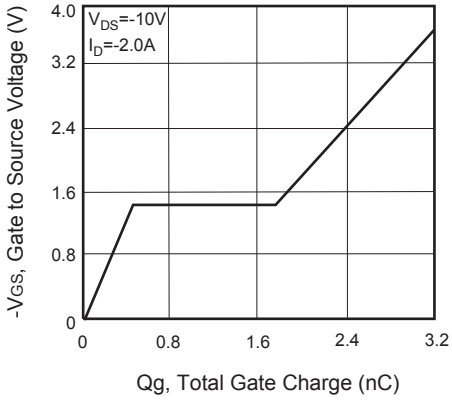

Figure 15. Gate Charge

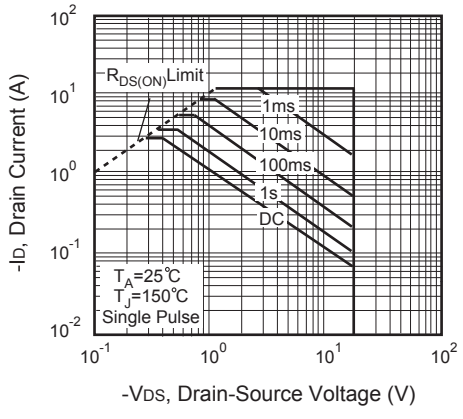

Figure 16. Maximum Safe Operating Area

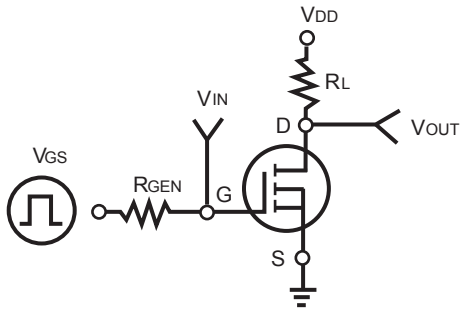

Figure 17. Switching Test Circuit

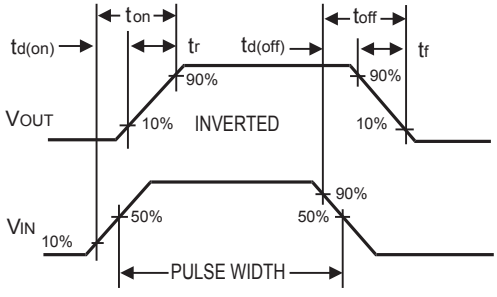

Figure 18. Switching Waveforms

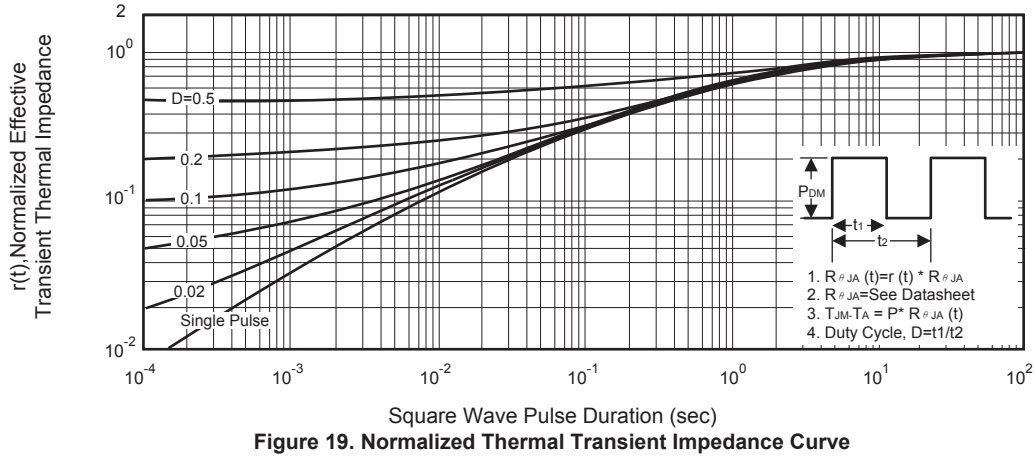

Figure 19. Normalized Thermal Transient Impedance Curve