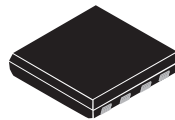
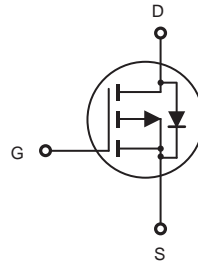


## Dual P-Channel Enhancement Mode Field Effect Transistor

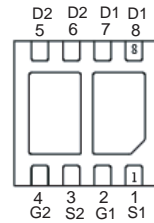
PRELIMINARY

### FEATURES

- -30V, -17A,  $R_{DS(ON)} = 25m\Omega @V_{GS} = -10V$ .  
 $R_{DS(ON)} = 32m\Omega @V_{GS} = -4.5V$ .
- Super High dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- RoHS compliant.



DFN3\*3



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

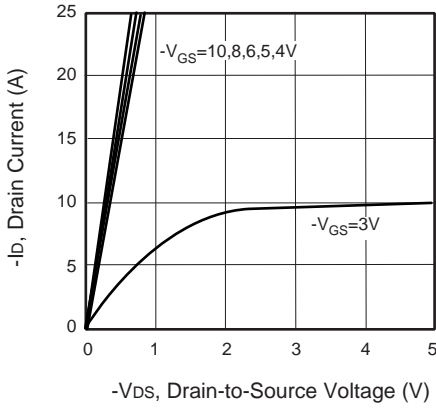
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$R_{\theta jc} = 25^\circ\text{C}$	$I_D$	-17	A
	$R_{\theta jc} = 100^\circ\text{C}$		-11	A
	$R_{\theta JA} = 25^\circ\text{C}$		-8	A
	$R_{\theta JA} = 100^\circ\text{C}$		-5	A
Drain Current-Pulsed <sup>a</sup>	$R_{\theta jc} = 25^\circ\text{C}$	$I_{DM}$	-68	A
	$R_{\theta JA} = 25^\circ\text{C}$		-32	A
Maximum Power Dissipation	$R_{\theta jc} = 25^\circ\text{C}$	$P_D$	12.5	W
	$R_{\theta JA} = 25^\circ\text{C}$		2.5	W
Operating and Store Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

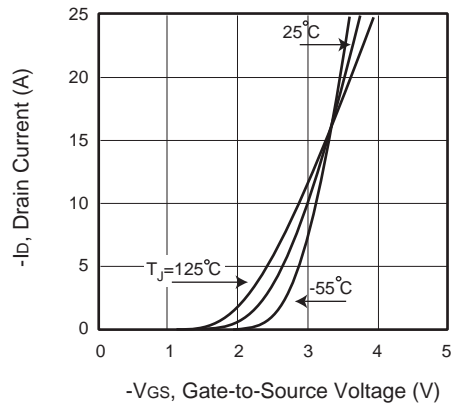
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case <sup>b</sup>	$R_{\theta jc}$	10	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	50	$^\circ\text{C/W}$

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

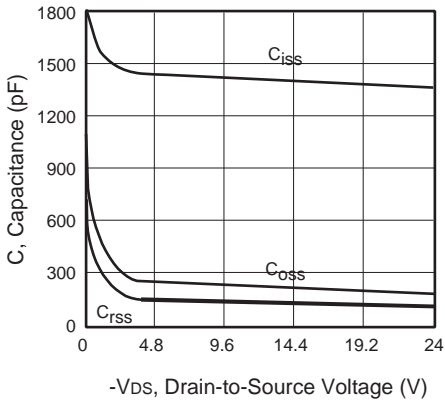
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -8A$		20	25	$m\Omega$
		$V_{GS} = -4.5V, I_D = -8A$		24	32	$m\Omega$
<b>Dynamic Characteristics <sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -24V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		1385		pF
Output Capacitance	$C_{oss}$			185		pF
Reverse Transfer Capacitance	$C_{rss}$			135		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -24V, I_D = -8A,$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		20		ns
Turn-On Rise Time	$t_r$			8		ns
Turn-Off Delay Time	$t_{d(off)}$			66		ns
Turn-Off Fall Time	$t_f$			14		ns
Total Gate Charge	$Q_g$	$V_{DS} = -24V, I_D = -8A,$ $V_{GS} = -4.5V$		16		nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				-10	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -1A$			-1.2	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec.}$ □ c.Pulse Test : Pulse Width $\leq 300\mu s,$ Duty Cycle $\leq 2\%.$ □ d.Guaranteed by design, not subject to production testing. □						



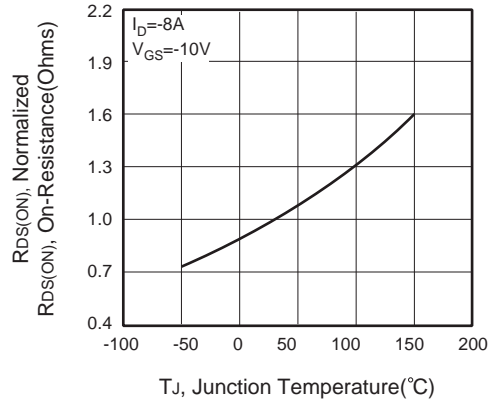
**Figure 1. Output Characteristics**



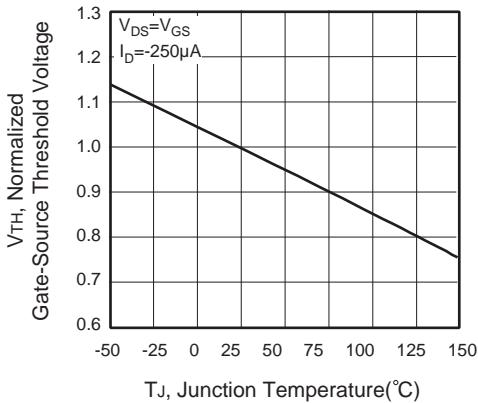
**Figure 2. Transfer Characteristics**



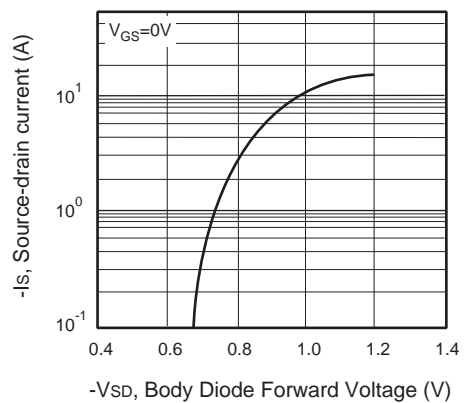
**Figure 3. Capacitance**



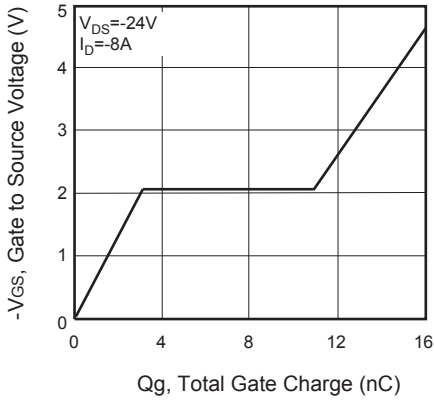
**Figure 4. On-Resistance Variation with Temperature**



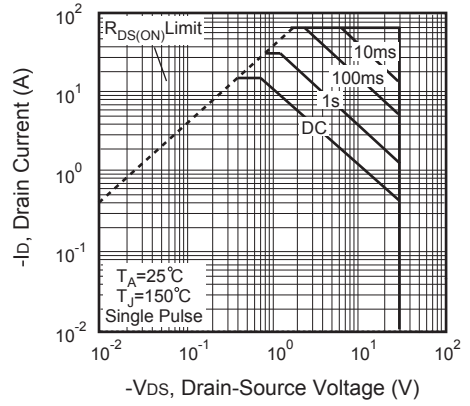
**Figure 5. Gate Threshold Variation with Temperature**



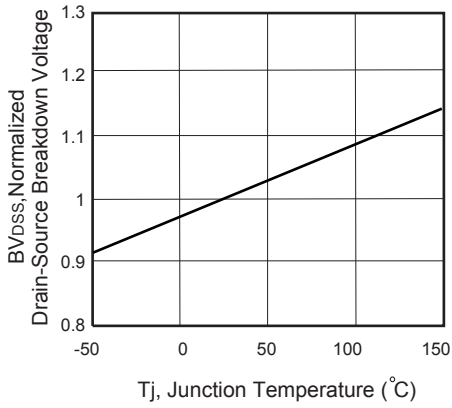
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



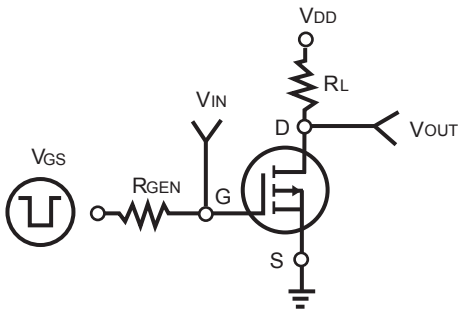
**Figure 7. Gate Charge**



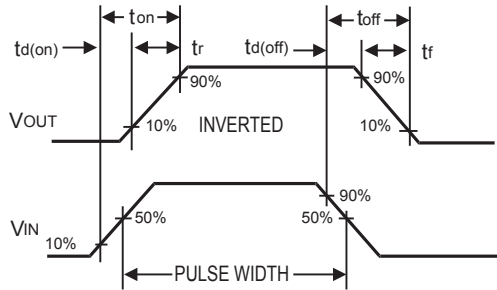
**Figure 8. Maximum Safe Operating Area**



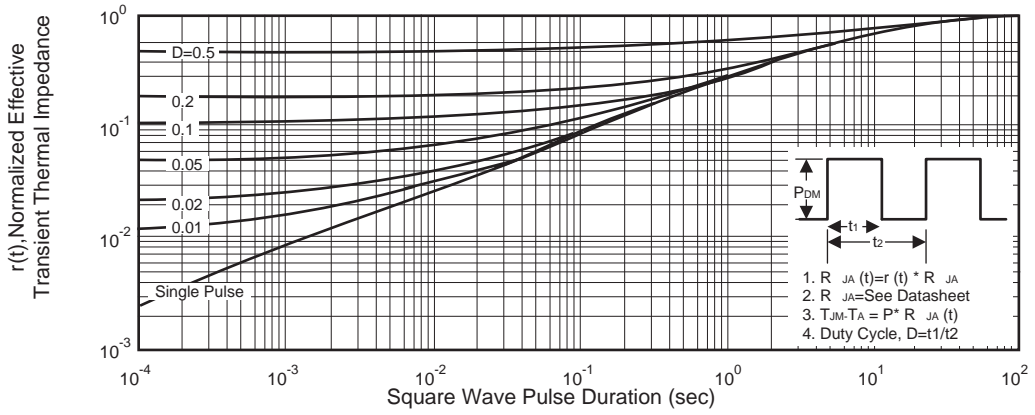
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**



**Figure 12. Normalized Thermal Transient Impedance Curve**