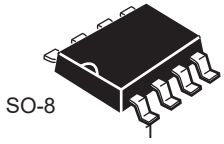
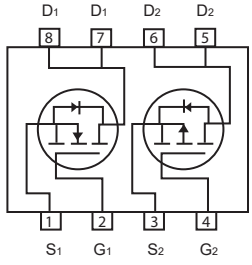
CEM3119A

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 20V, 9A, $R_{DS(ON)}$ = 15mΩ @V_{GS} = 4.5V.
  $R_{DS(ON)}$ = 19mΩ @V_{GS} = 2.5V.
- -30V, -8.3A, $R_{DS(ON)}$ = 18mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 26mΩ @V_{GS} = -4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.
- Surface mount Package.





ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	20	-30	V
Gate-Source Voltage	V_{GS}	±12	±25	V
Drain Current-Continuous	I_D	9	-8.3	A
Drain Current-Pulsed [a]	I_{DM}	36	-33.2	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics [a] T_A = 25 C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	0.4		1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 8A		12	15	mΩ
		V_{GS} = 2.5V, I_D = 5A		14.5	19	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V, f = 1.0 MHz		1305		pF
Output Capacitance	C_{oss}			135		pF
Reverse Transfer Capacitance	C_{rss}			105		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, R_L = 1.8Ω, V_{GS} = 10V, R_{GEN} = 3Ω		9		ns
Turn-On Rise Time	t_r			3		ns
Turn-Off Delay Time	$t_{d(off)}$			40		ns
Turn-Off Fall Time	t_f			3		ns
Total Gate Charge	Q_g	V_{DS} = 15V, I_D = 8A, V_{GS} = 10V		29		nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			3		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics [a] T_A = 25 C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-0.8		-2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -4A		14	18	mΩ
		V_{GS} = -4.5V, I_D = -2A		21	26	mΩ
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		1710		pF
Output Capacitance	C_{oss}			260		pF
Reverse Transfer Capacitance	C_{rss}			185		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -24V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6Ω		16		ns
Turn-On Rise Time	t_r			8		ns
Turn-Off Delay Time	$t_{d(off)}$			75		ns
Turn-Off Fall Time	t_f			36		ns
Total Gate Charge	Q_g	V_{DS} = -24V, I_D = -1A, V_{GS} = -4.5V		18		nC
Gate-Source Charge	Q_{gs}			3.4		nC
Gate-Drain Charge	Q_{gd}			7.1		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				-1.6	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

N-CHANNEL

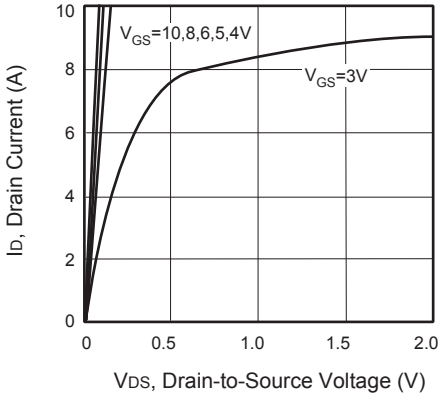


Figure 1. Output Characteristics

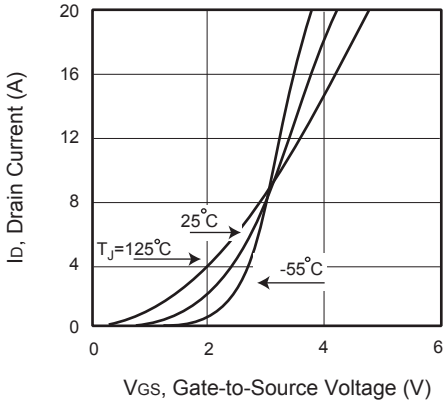


Figure 2. Transfer Characteristics

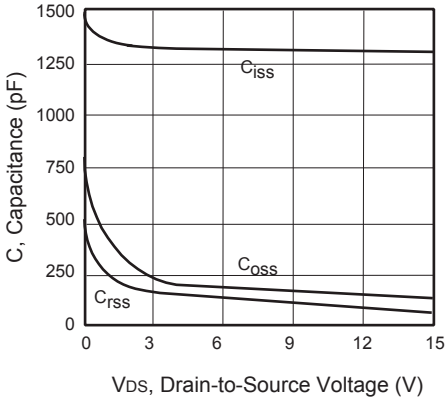


Figure 3. Capacitance

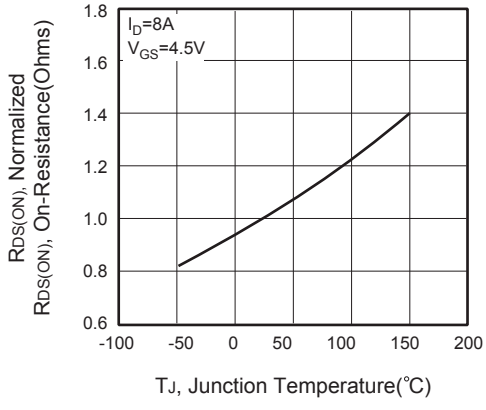


Figure 4. On-Resistance Variation with Temperature

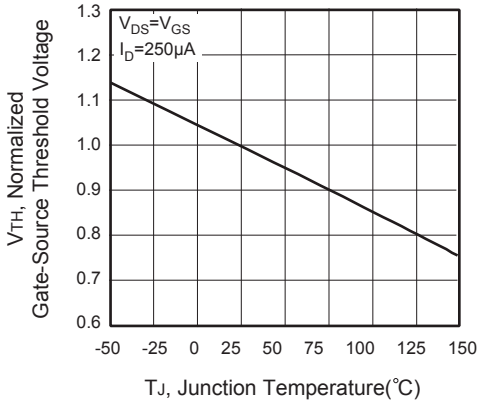


Figure 5. Gate Threshold Variation with Temperature

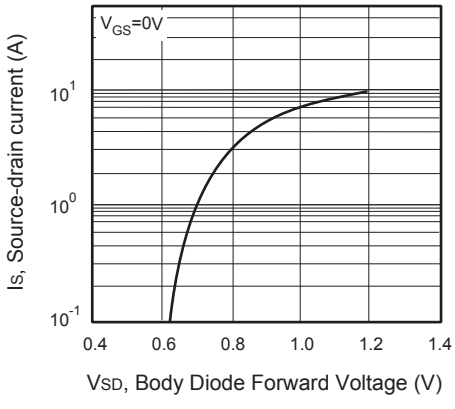


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

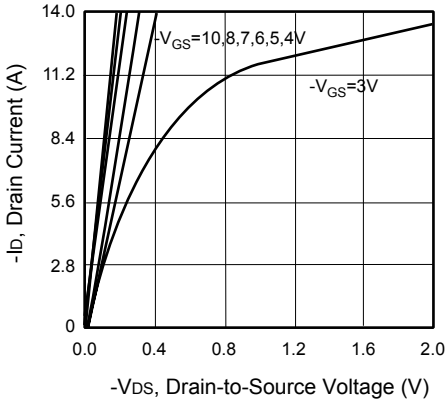


Figure 1. Output Characteristics

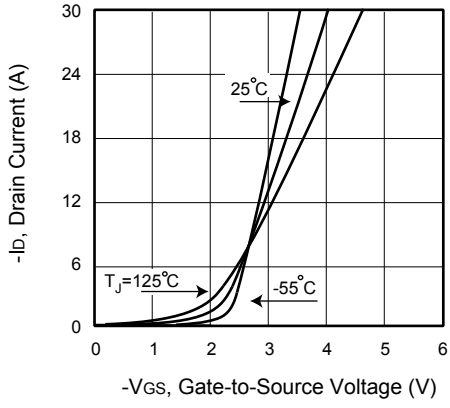


Figure 2. Transfer Characteristics

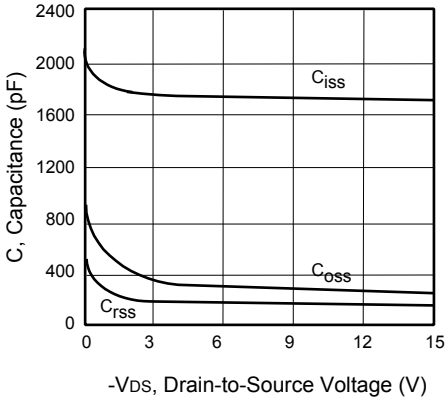


Figure 3. Capacitance

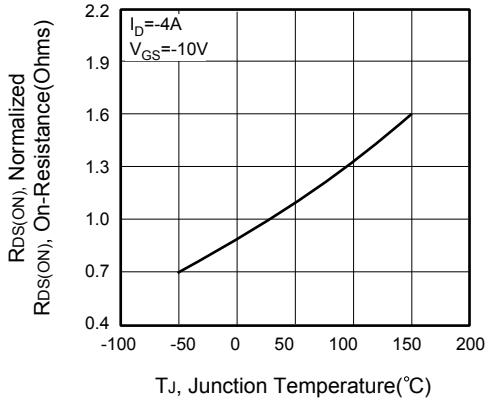


Figure 4. On-Resistance Variation with Temperature

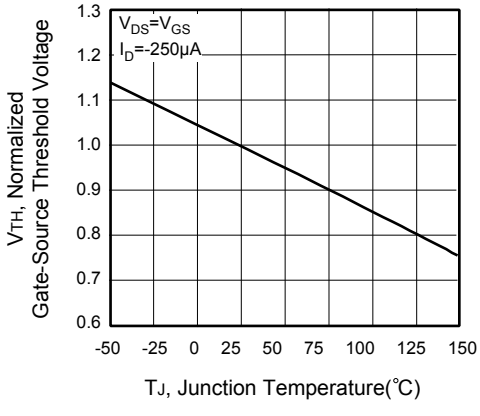


Figure 5. Gate Threshold Variation with Temperature

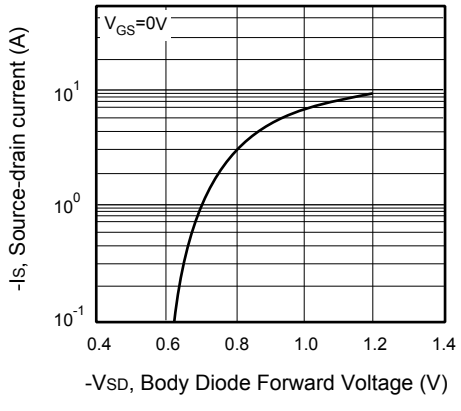


Figure 6. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

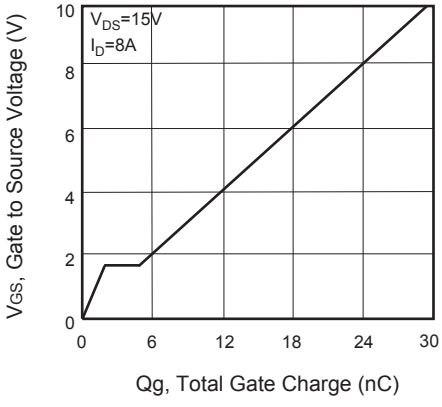


Figure 13. Gate Charge

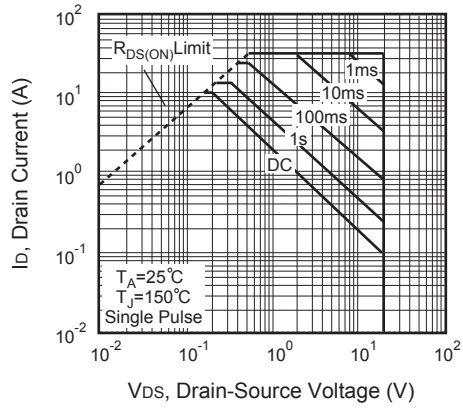


Figure 14. Maximum Safe Operating Area

P-CHANNEL

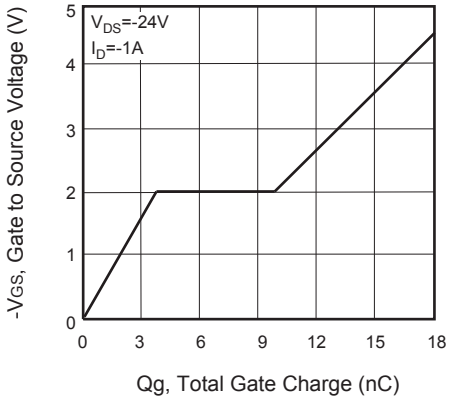


Figure 15. Gate Charge

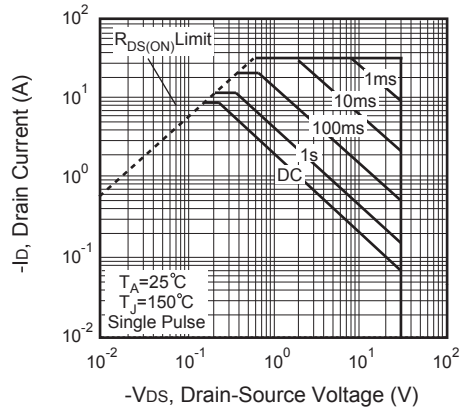


Figure 16. Maximum Safe Operating Area

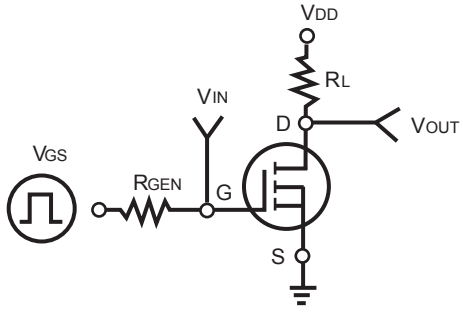


Figure 17. Switching Test Circuit

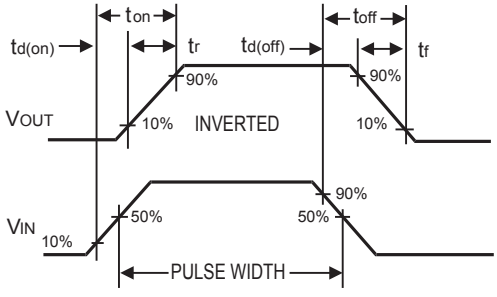


Figure 18. Switching Waveforms

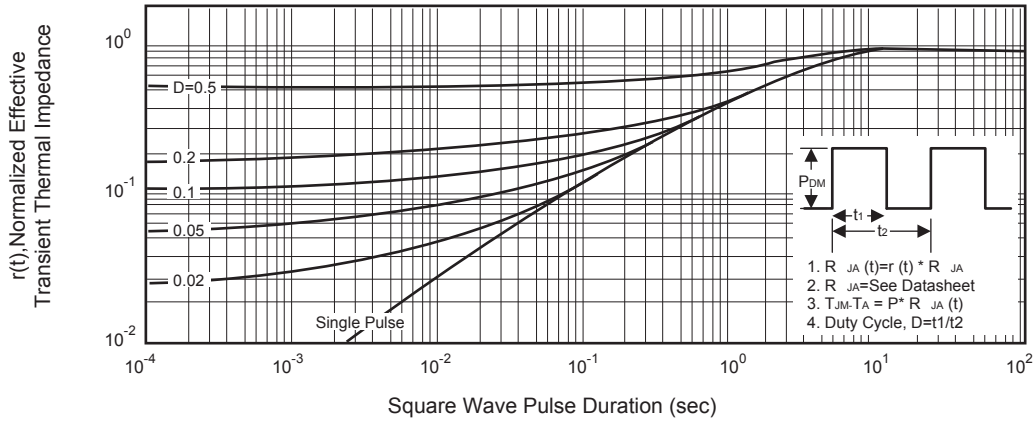


Figure 19. Normalized Thermal Transient Impedance Curve