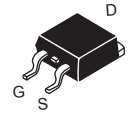
CEP13N5/CEB13N5
CEF13N5

N-Channel Enhancement Mode Field Effect Transistor

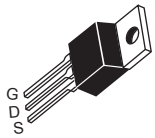
FEATURES

Type	V_{DSS}	$R_{DS(ON)}$	I_D	@V_{GS}
CEP13N5	500V	0.48Ω	13A	10V
CEB13N5	500V	0.48Ω	13A	10V
CEF13N5	500V	0.48Ω	13A [d]	10V

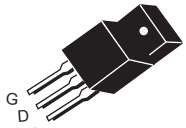
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.



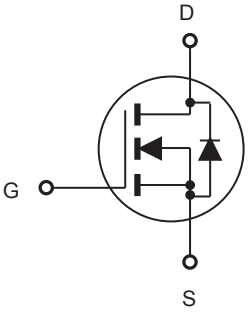
CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	500		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current-Continuous @ T_C = 25°C	I_D	13	13 [d]	A
Drain Current-Continuous @ T_C = 100°C	I_D	8	8 [d]	A
Drain Current-Pulsed [a]	I_{DM} [e]	52	52[d]	A
Maximum Power Dissipation @ T_C = 25°C	P_D	214	60	W
- Derate above 25°C		1.43	0.4	W/°C
Single Pulsed Avalanche Energy [h]	E_{AS}	781		mJ
Single Pulsed Avalanche Current [h]	I_{AS}	12.5		A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	RθJC	0.7	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	RθJA	62.5	65	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =500V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 30V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -30V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6.5A		0.38	0.48	Ω
Forward Transconductance	g_{FS}	V_{DS} = 25V, I_D =6.5A		10		S
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		2100		pF
Output Capacitance	C_{oss}			220		pF
Reverse Transfer Capacitance	C_{rss}			7		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250V, I_D =13A, V_{GS} = 10V, R_{GEN} = 25Ω		42	84	ns
Turn-On Rise Time	t_r			62	124	ns
Turn-Off Delay Time	$t_{d(off)}$			130	260	ns
Turn-Off Fall Time	t_f			25	50	ns
Total Gate Charge	Q_g	V_{DS} = 400V,I_D = 13A, V_{GS} = 10V		50	66	nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			19		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S [f]				13	A
Drain-Source Diode Forward Voltage [b]	V_{SD} [g]	V_{GS} = 0V, I_S = 13A			1.4	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature .
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2% .
c.Guaranteed by design, not subject to production testing.
d.Limited only by maximum temperature allowed .
e.Pulse width limited by safe operating area .
f.Full package $I_{S(max)}$ =6.6A .
g.Full package V_{SD} test condition I_S =6.6A .
h.Vdd=50V L=10mH Ias=12.5A

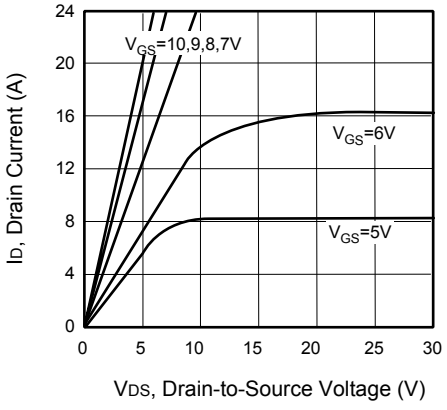


Figure 1. Output Characteristics

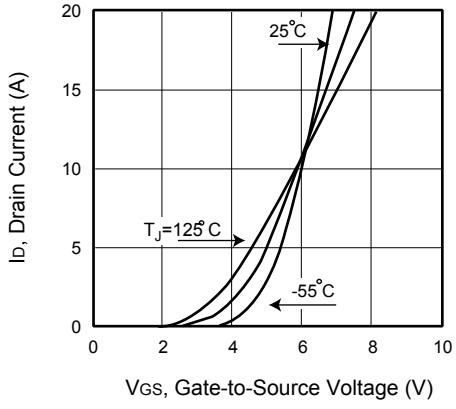


Figure 2. Transfer Characteristics

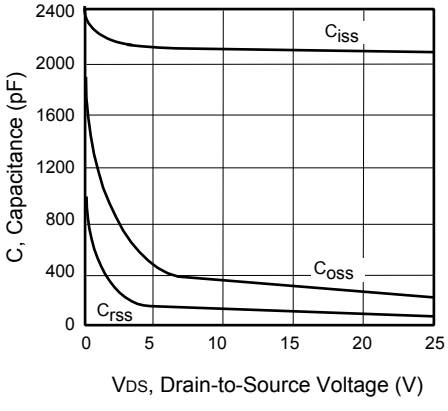


Figure 3. Capacitance

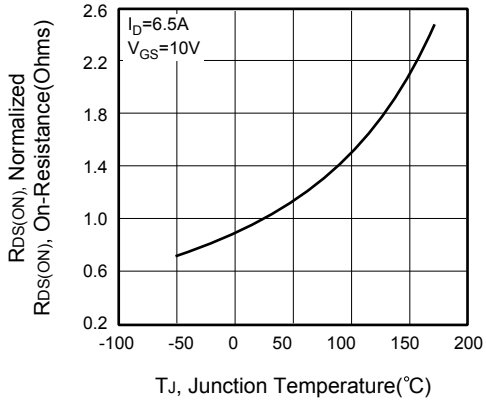


Figure 4. On-Resistance Variation with Temperature

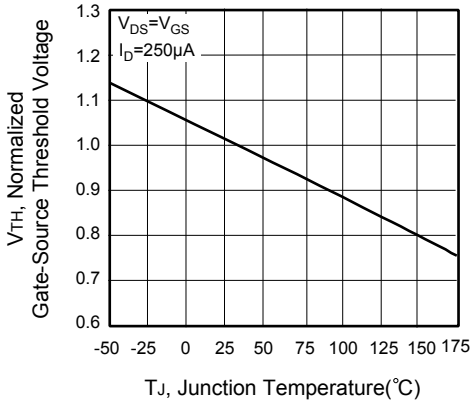


Figure 5. Gate Threshold Variation with Temperature

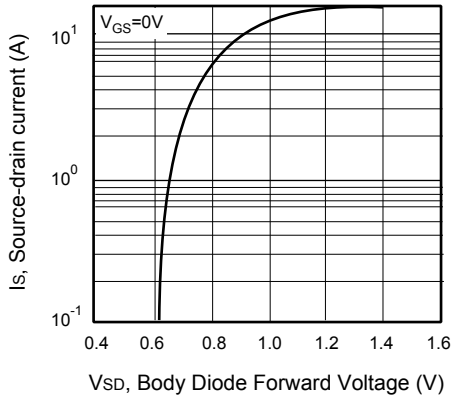


Figure 6. Body Diode Forward Voltage Variation with Source Current

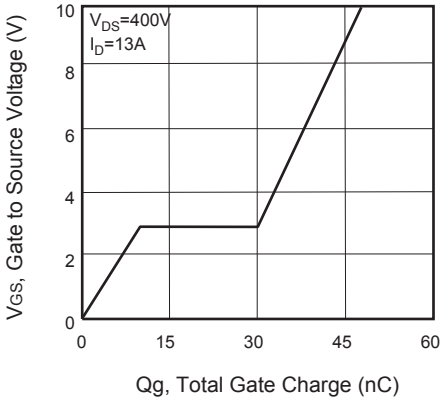


Figure 7. Gate Charge

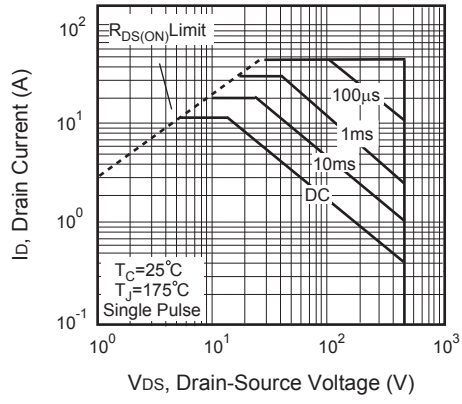


Figure 8. Maximum Safe Operating Area

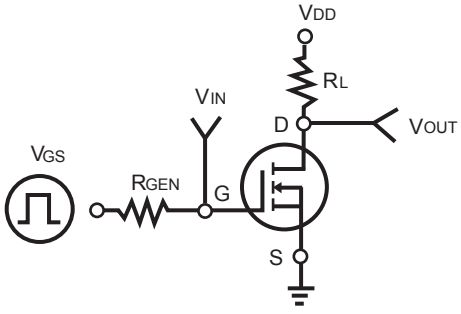


Figure 9. Switching Test Circuit

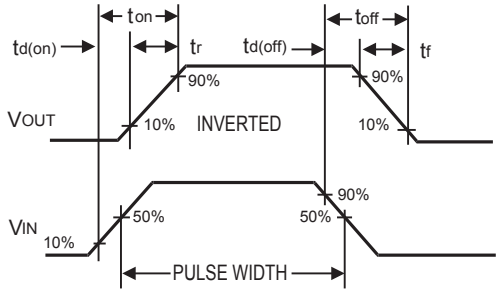


Figure 10. Switching Waveforms

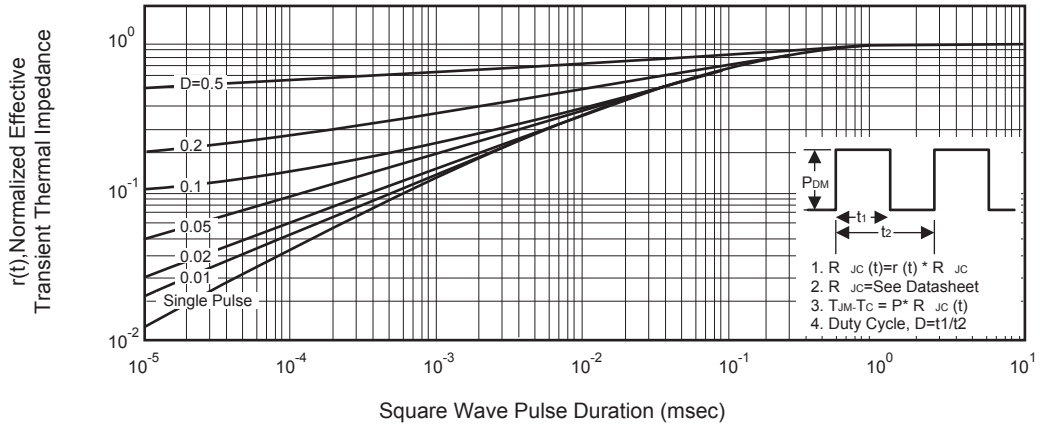


Figure 11. Normalized Thermal Transient Impedance Curve