



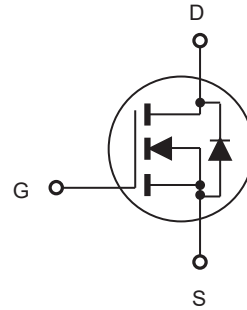
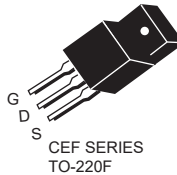
# CEP38N65SA/CEB38N65SA CEF38N65SA

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP38N65SA	650V	0.095Ω	39A	10V
CEB38N65SA	650V	0.095Ω	39A	10V
CEF38N65SA	650V	0.095Ω	39A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	650		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	39	39 <sup>d</sup>	A
		24.5	24.5 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	155.2	155.2 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	357	89	W
		2.9	0.7	W/°C
Single Pulsed Avalanche Energy <sup>h</sup>	E <sub>AS</sub>	735		mJ
Single Pulsed Avalanche Current <sup>h</sup>	I <sub>AS</sub>	7		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.35	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



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## CEF38N65SA

### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.5		4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		0.08	0.095	$\Omega$
Gate input resistance	$R_g$	$f=1\text{MHz, open Drain}$		3.3		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 150V, V_{GS} = 0V, f = 1.0 \text{ MHz}$		1915		pF
Output Capacitance	$C_{oss}$			110		pF
Reverse Transfer Capacitance	$C_{rss}$			5		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520V, I_D = 20A, V_{GS} = 10V, R_{GEN} = 6\Omega$		37		ns
Turn-On Rise Time	$t_r$			17		ns
Turn-Off Delay Time	$t_{d(off)}$			95		ns
Turn-Off Fall Time	$t_f$			9		ns
Total Gate Charge	$Q_g$	$V_{DS} = 520V, I_D = 20A, V_{GS} = 10V$		69		nC
Gate-Source Charge	$Q_{gs}$			12		nC
Gate-Drain Charge	$Q_{gd}$			30		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				39	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 20A^g$			1.5	V
Reverse Recovery Time	$T_{rr}$	$V_R = 25V, I_F = 10A, di_F/dt = 100A/\mu s$		324		ns
Reverse Recovery Charge	$Q_{rr}$			4.2		$\mu C$
Maximum diode commutation speed	$di_F/dt$	$V_{DS} = 0 \dots 400V, I_{SD} < 20A, T_J = 25^\circ C$			1300	A/ $\mu s$
<b>Notes :</b> a. Repetitive Rating : Pulse width limited by maximum junction temperature . b. Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c. Guaranteed by design, not subject to production testing. d. Limited only by maximum temperature allowed . e. Pulse width limited by safe operating area . f. Full package $I_{S(max)} = 19A$ . g. Full package $V_{SD}$ test condition $I_S = 19A$ . h. $L = 30mH, I_{AS} = 7A, V_{DD} = 60V, R_G = 25\Omega$ , Starting $T_J = 25^\circ C$ .						



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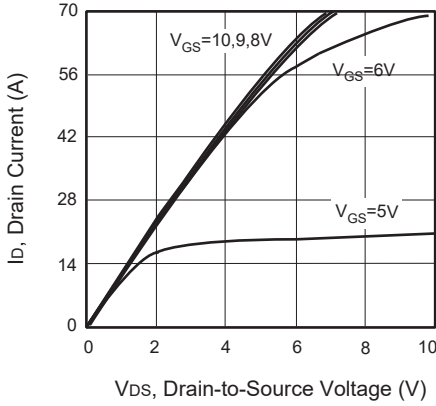


Figure 1. Output Characteristics

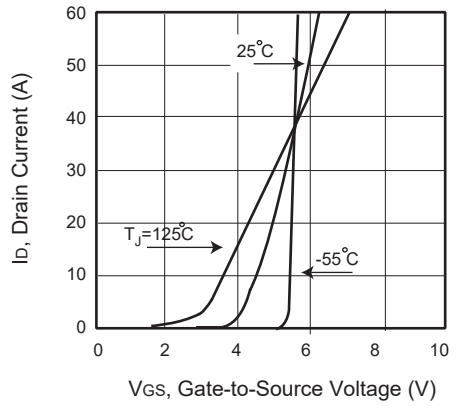


Figure 2. Transfer Characteristics

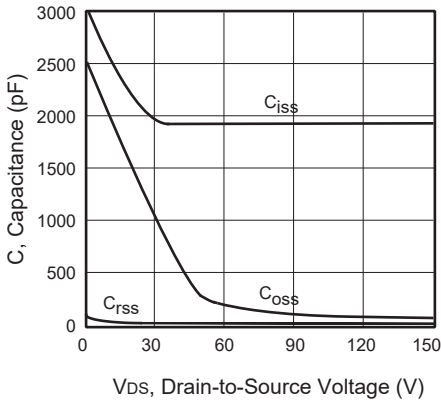


Figure 3. Capacitance

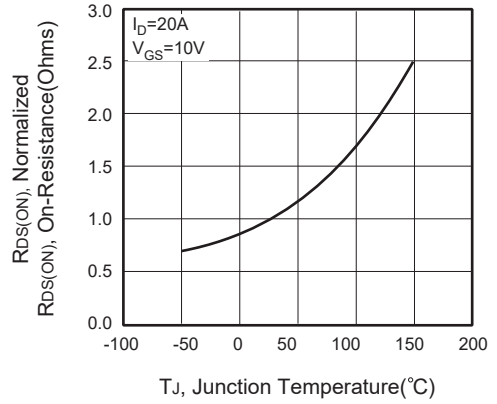


Figure 4. On-Resistance Variation with Temperature

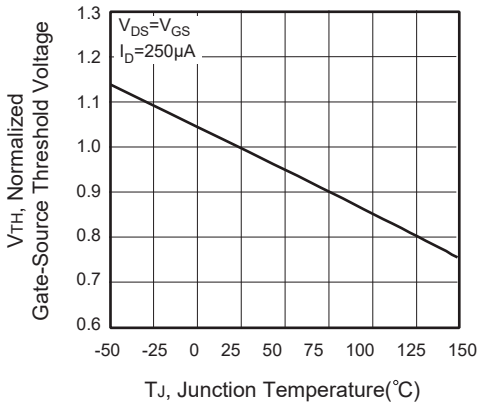


Figure 5. Gate Threshold Variation with Temperature

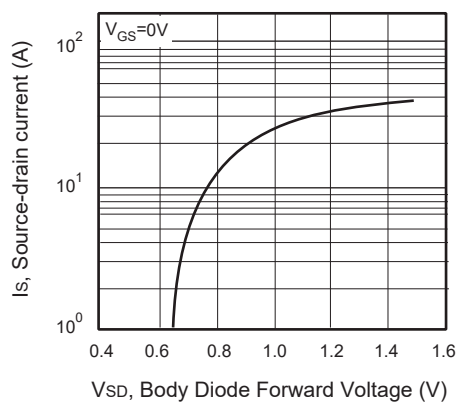


Figure 6. Body Diode Forward Voltage Variation with Source Current



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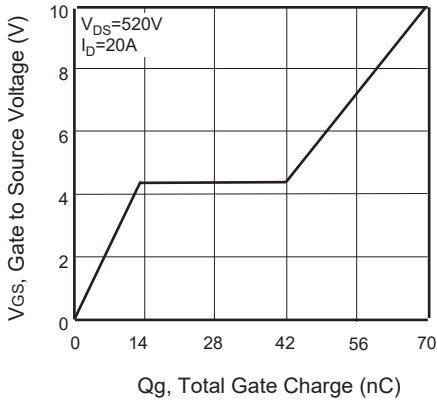


Figure 7. Gate Charge

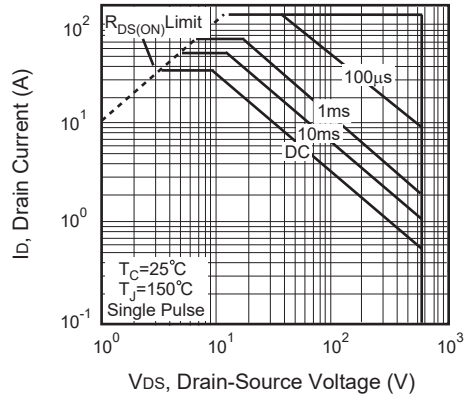


Figure 8. Maximum Safe Operating Area

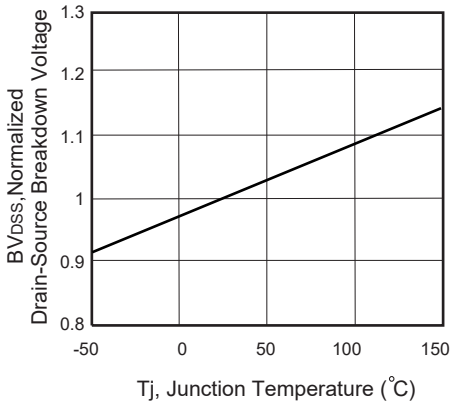


Figure 9. Breakdown Voltage Variation VS Temperature

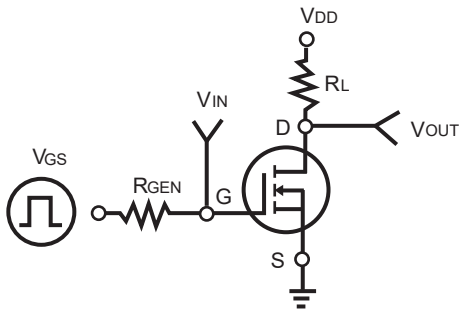


Figure 10. Switching Test Circuit

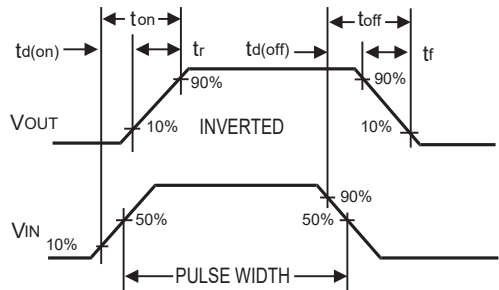


Figure 11. Switching Waveforms



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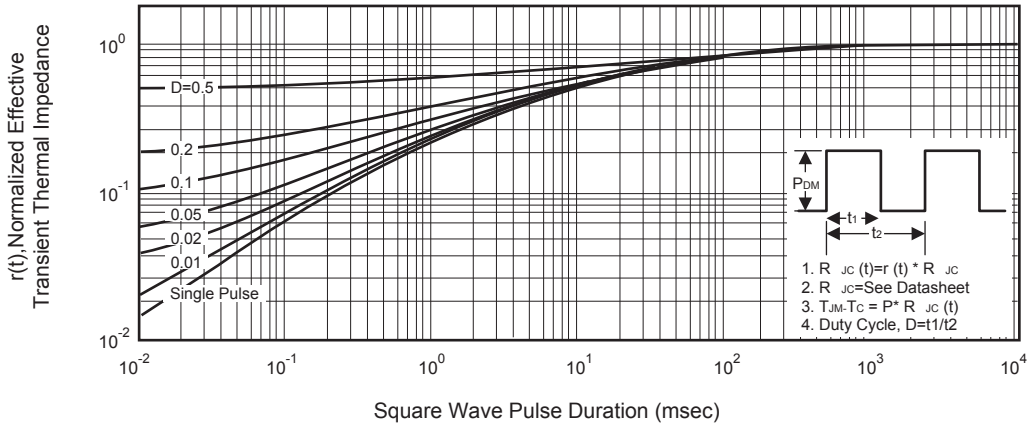


Figure 12. Normalized Thermal Transient Impedance Curve