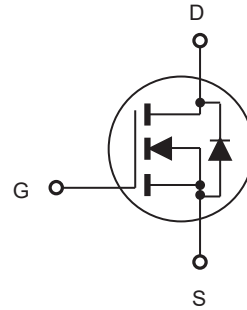
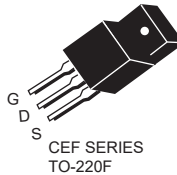


N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP45N65S	650V	70mΩ	45A	10V
CEB45N65S	650V	70mΩ	45A	10V
CEF45N65S	650V	70mΩ	45A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	650		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous @ T _C = 25°C @ T _C = 100°C	I _D	45	45 ^d	A
		28	28 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	180	180 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	357	89	W
		2.8	0.7	W/°C
Single Pulsed Avalanche Energy ^h	E _{AS}	300		mJ
Single Pulsed Avalanche Current ^h	I _{AS}	4		A
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	0.35	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W



CEP45N65S/CEB45N65S CEF45N65S

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.5		4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		56	70	m Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		2905		pF
Output Capacitance	C_{oss}			160		pF
Reverse Transfer Capacitance	C_{rss}			5		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 10\Omega$		42		ns
Turn-On Rise Time	t_r			21		ns
Turn-Off Delay Time	$t_{d(off)}$			124		ns
Turn-Off Fall Time	t_f			5		ns
Total Gate Charge	Q_g	$V_{DS} = 520V, I_D = 10A,$ $V_{GS} = 10V$		79		nC
Gate-Source Charge	Q_{gs}			18		nC
Gate-Drain Charge	Q_{gd}			25		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				45	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 20A^g$			1.5	V
Reverse Recovery Time	T_{rr}	$V_R = 400V, I_F = 23A,$ $dI_F/dt = 100A/\mu s$		386		ns
Reverse Recovery Charge	Q_{rr}			8.7		nC
Peak Reverse Recovery Current	I_{rrm}			44.2		A
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width < 300 μs , Duty Cycle < 2% . c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 22A$. g.Full package V_{SD} test condition $I_S = 22A$. h.L = 37.5mH, $I_{AS} = 4A, V_{DD} = 60V, R_G = 25\Omega$, Starting $T_J = 25\text{ C}$.						



CEP45N65S/CEB45N65S CEF45N65S

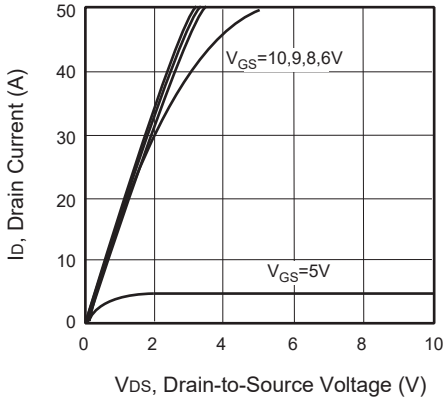


Figure 1. Output Characteristics

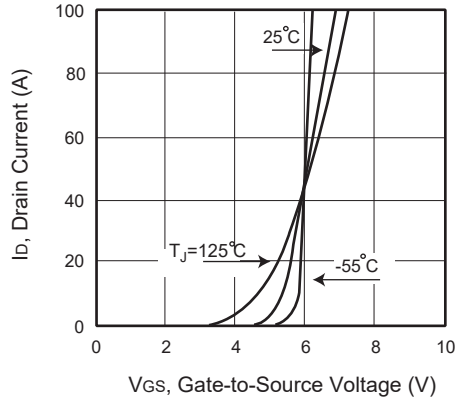


Figure 2. Transfer Characteristics

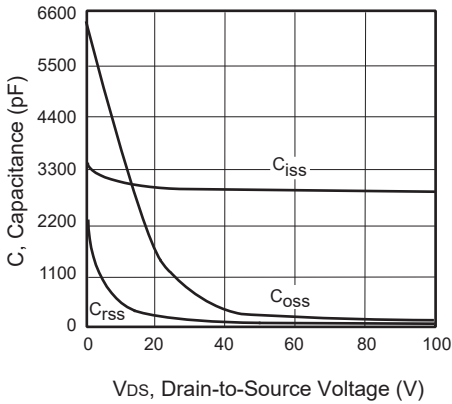


Figure 3. Capacitance

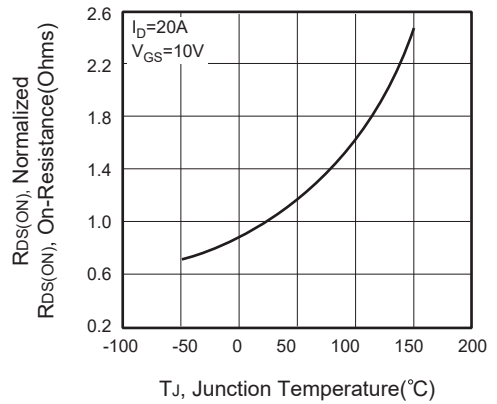


Figure 4. On-Resistance Variation with Temperature

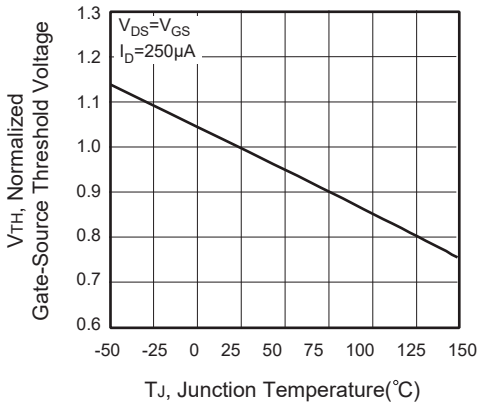


Figure 5. Gate Threshold Variation with Temperature

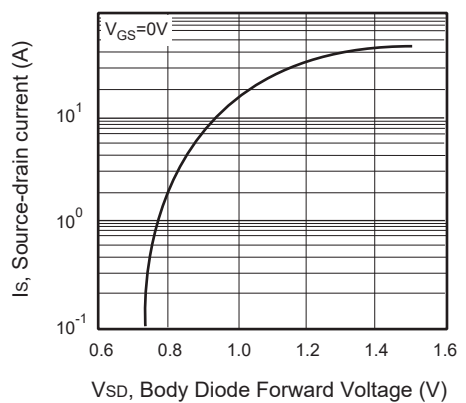


Figure 6. Body Diode Forward Voltage Variation with Source Current

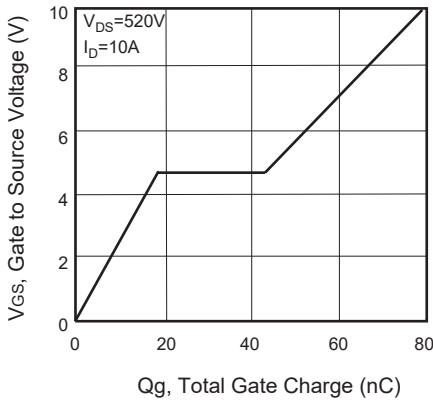


Figure 7. Gate Charge

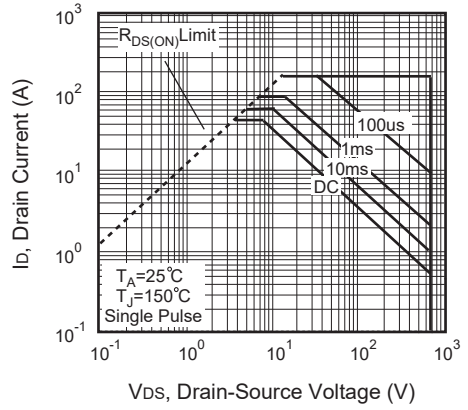


Figure 8. Maximum Safe Operating Area

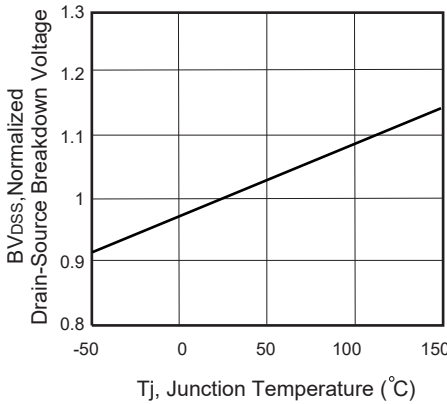


Figure 9. Breakdown Voltage Variation VS Temperature

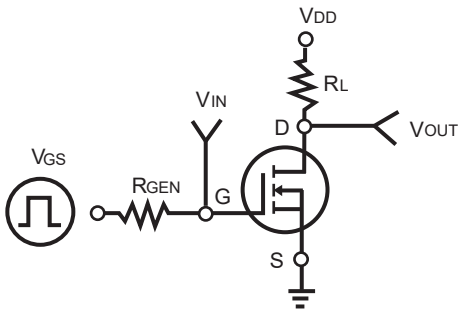


Figure 10. Switching Test Circuit

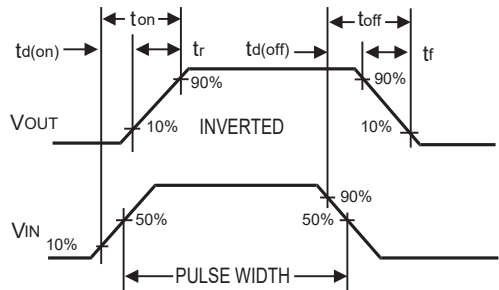


Figure 11. Switching Waveforms



CEP45N65S/CEB45N65S CEF45N65S

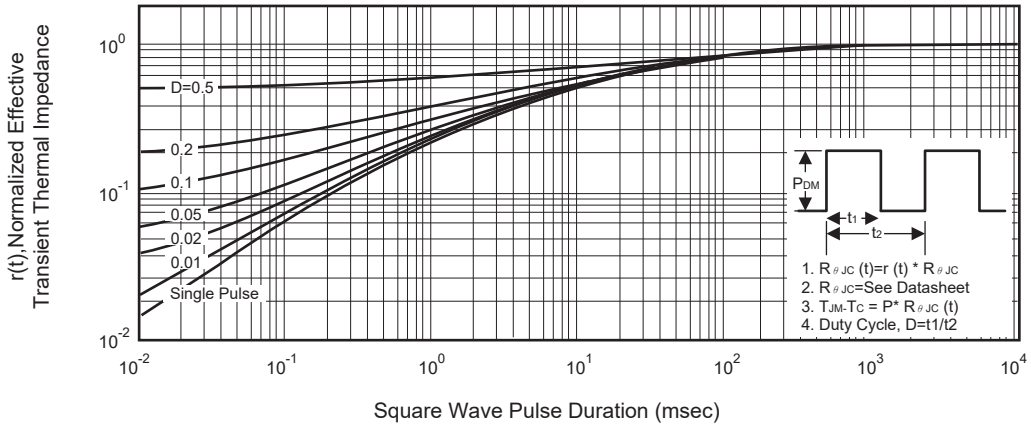


Figure 12. Normalized Thermal Transient Impedance Curve