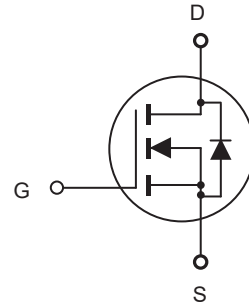


# CET CED15N60SA/CEU15N60SA

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 650V@ $T_{J\max}$ , 13.4A,  $R_{DS(ON)} = 0.28\Omega$  @ $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- RoHS compliant.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$I_D$	13.4	A
		8.5	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	53.6	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	125	W
		1	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>e</sup>	$E_{AS}$	400	mJ
Single Pulsed Avalanche Current <sup>e</sup>	$I_{AS}$	4	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

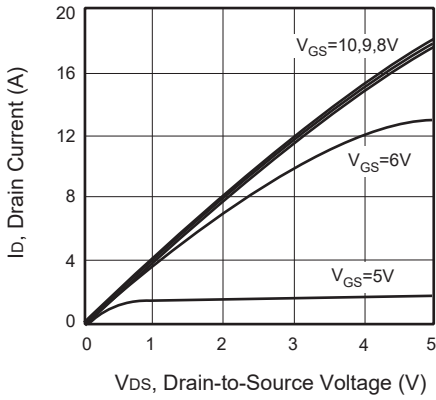
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$



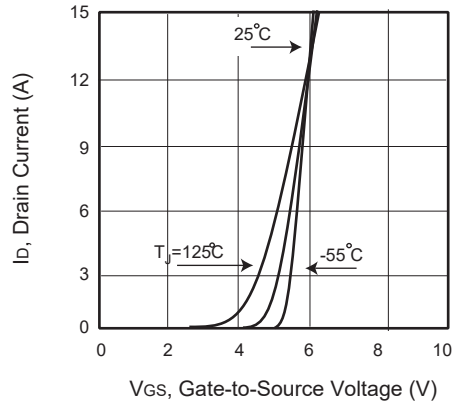
# CED15N60SA/CEU15N60SA

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

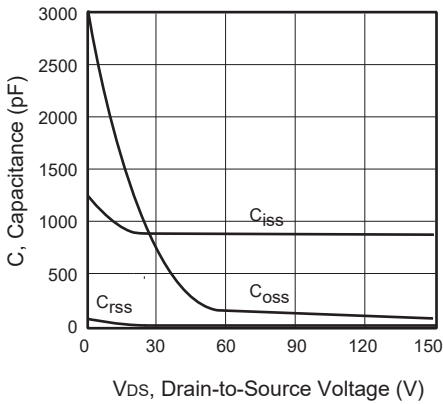
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	600			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics</b> <sup>c</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.5		4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 7.5A$		0.24	0.28	$\Omega$
<b>Dynamic Characteristics</b> <sup>d</sup>						
Input Capacitance	$C_{iss}$	$V_{DS} = 150V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		870		pF
Output Capacitance	$C_{oss}$			65		pF
Reverse Transfer Capacitance	$C_{rss}$			10		pF
<b>Switching Characteristics</b> <sup>d</sup>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 7.5A,$ $V_{GS} = 15V, R_{GEN} = 10\Omega$		26		ns
Turn-On Rise Time	$t_r$			7		ns
Turn-Off Delay Time	$t_{d(off)}$			82		ns
Turn-Off Fall Time	$t_f$			10		ns
Total Gate Charge	$Q_g$	$V_{DS} = 400V, I_D = 1A,$ $V_{GS} = 10V$		25		nC
Gate-Source Charge	$Q_{gs}$			4		nC
Gate-Drain Charge	$Q_{gd}$			12		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				13.4	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 7.5A$			1.2	V
Reverse Recovery Time	$T_{rr}$	$I_F = 7.5A, di/dt = 100A/\mu s$		253		ns
Reverse Recovery Charge	$Q_{rr}$			2.71		$\mu C$
Peak Reverse Recovery Current	$I_{rr}$			17.7		A
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing. e.L = 50mH, $I_{AS} = 4A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ C$ .						



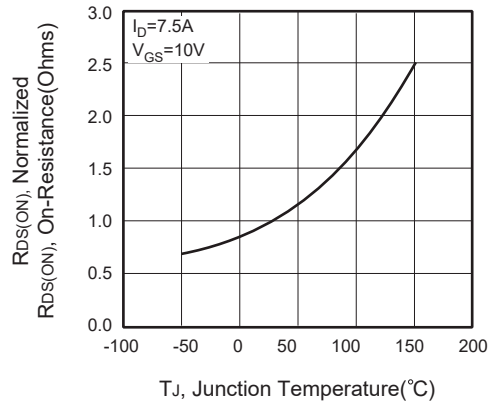
**Figure 1. Output Characteristics**



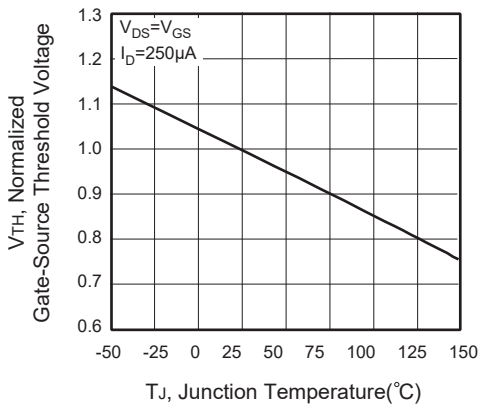
**Figure 2. Transfer Characteristics**



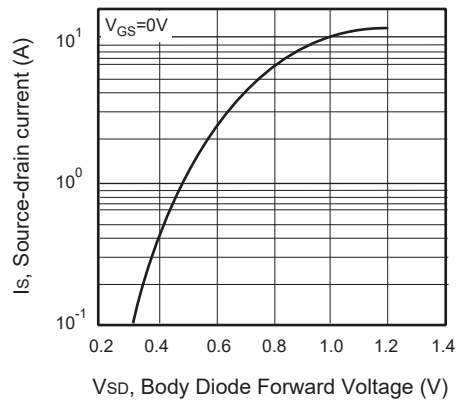
**Figure 3. Capacitance**



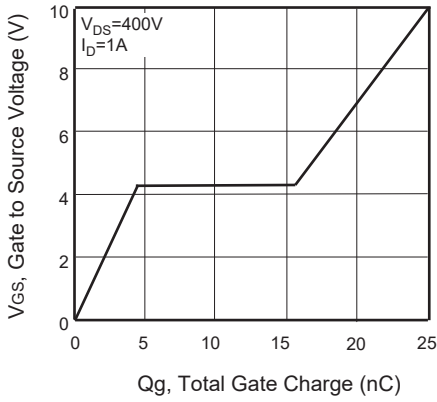
**Figure 4. On-Resistance Variation with Temperature**



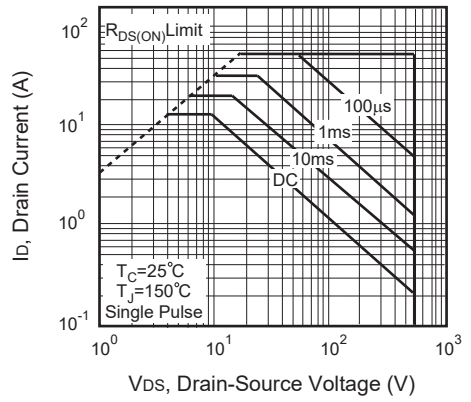
**Figure 5. Gate Threshold Variation with Temperature**



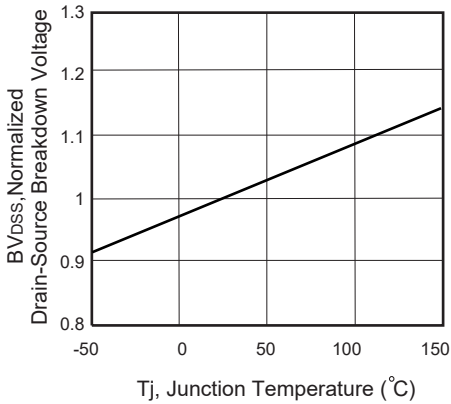
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



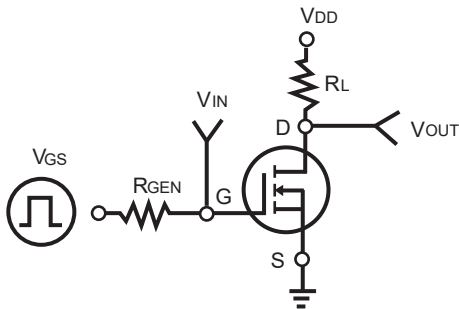
**Figure 7. Gate Charge**



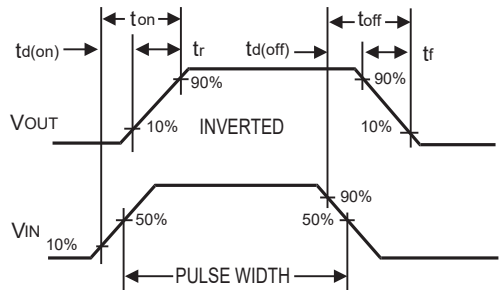
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**



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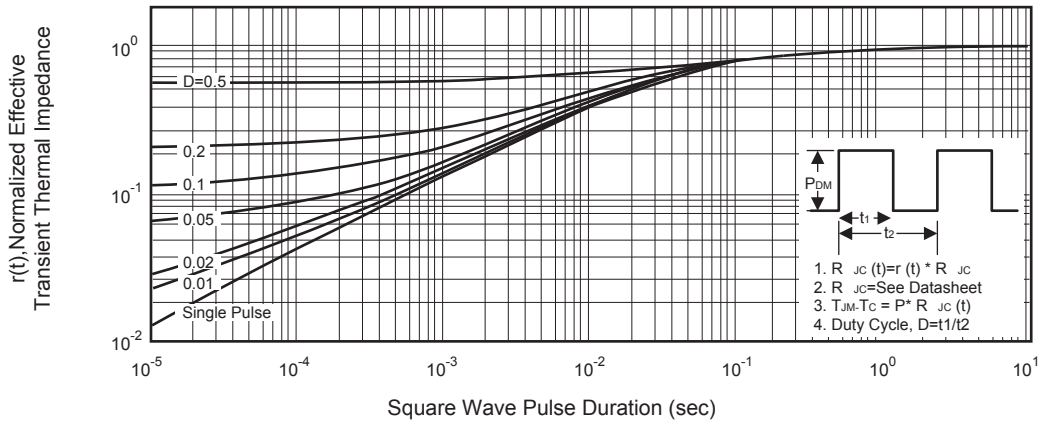


Figure 12. Normalized Thermal Transient Impedance Curve