

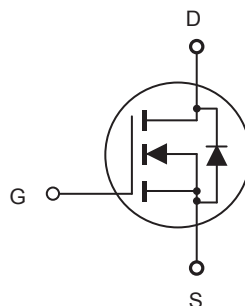


# CED4060AL/CEU4060AL

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 60V, 16A,  $R_{DS(ON)} = 75m\Omega$  @ $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 90m\Omega$  @ $V_{GS} = 5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	16	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	64	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	$P_D$	38	W
		0.25	W/ $^\circ C$
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ C$

### Thermal Characteristics

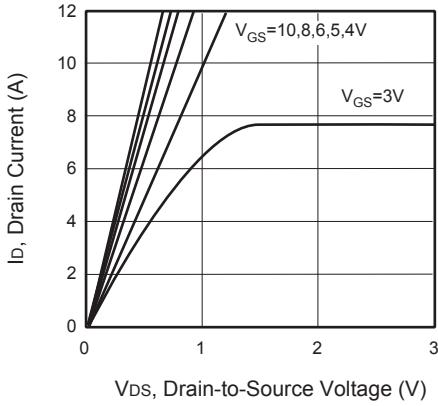
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ C/W$



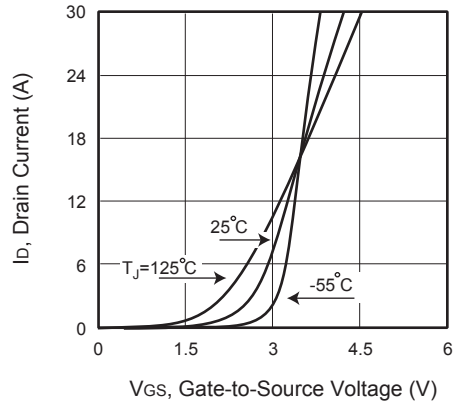
# CED4060AL/CEU4060AL

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

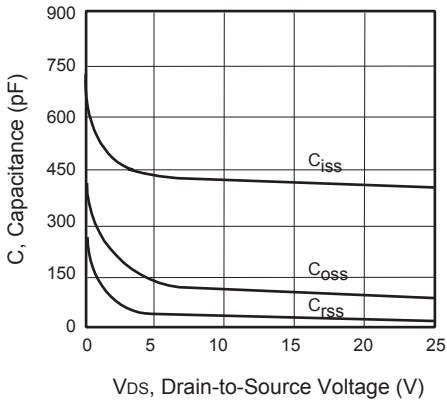
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0V$			25	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1	1.5	2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 12A$		60	75	$m\Omega$
		$V_{GS} = 5V, I_D = 6A$		70	90	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 6A$		10		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		405		pF
Output Capacitance	$C_{oss}$			120		pF
Reverse Transfer Capacitance	$C_{rss}$			30		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V, I_D = 15A, V_{GS} = 5V, R_{GEN} = 51\Omega$		10	13	ns
Turn-On Rise Time	$t_r$			7	9	ns
Turn-Off Delay Time	$t_{d(off)}$			84	110	ns
Turn-Off Fall Time	$t_f$			22	29	ns
Total Gate Charge	$Q_g$	$V_{DS} = 48V, I_D = 15A, V_{GS} = 10V$		12	17	nC
Gate-Source Charge	$Q_{gs}$			1.1		nC
Gate-Drain Charge	$Q_{gd}$			3.2		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				15	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 6A$		0.83	1.3	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . □ c.Guaranteed by design, not subject to production testing. □						



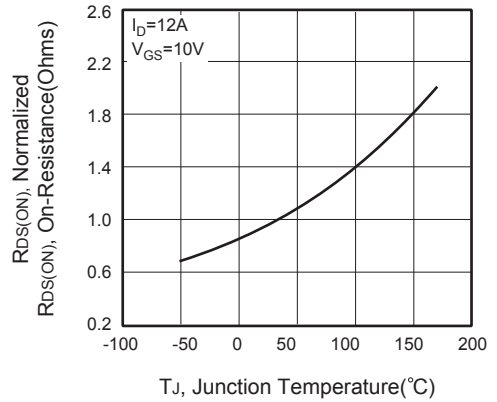
**Figure 1. Output Characteristics**



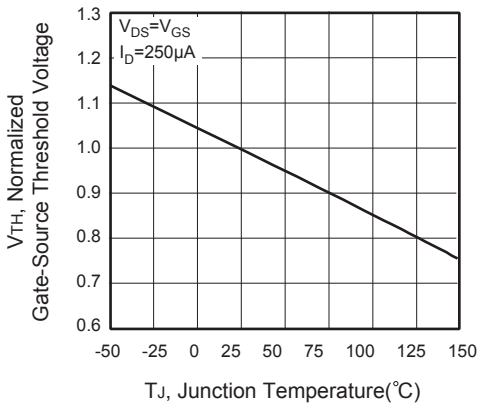
**Figure 2. Transfer Characteristics**



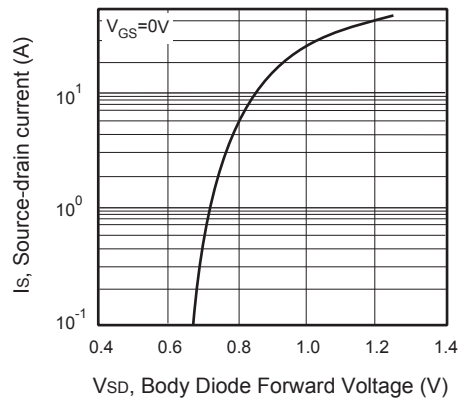
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

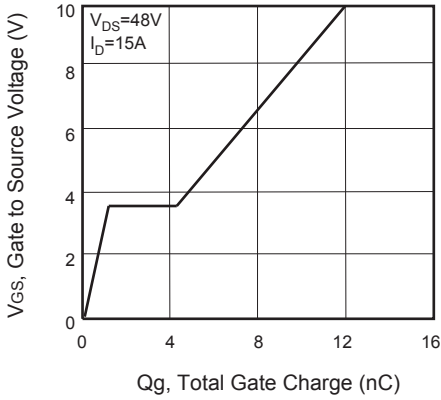


Figure 7. Gate Charge

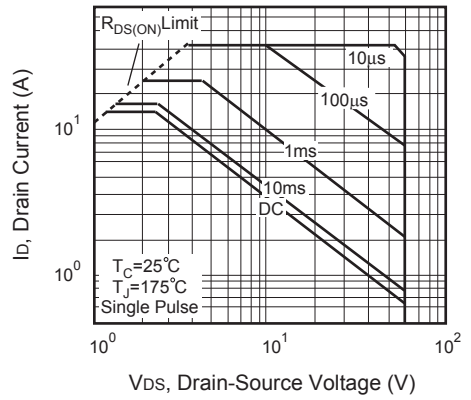


Figure 8. Maximum Safe Operating Area

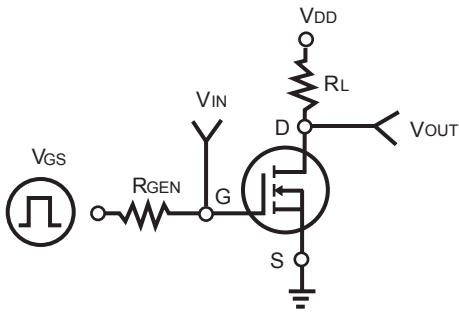


Figure 9. Switching Test Circuit

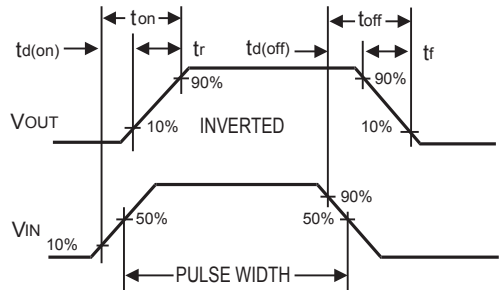


Figure 10. Switching Waveforms

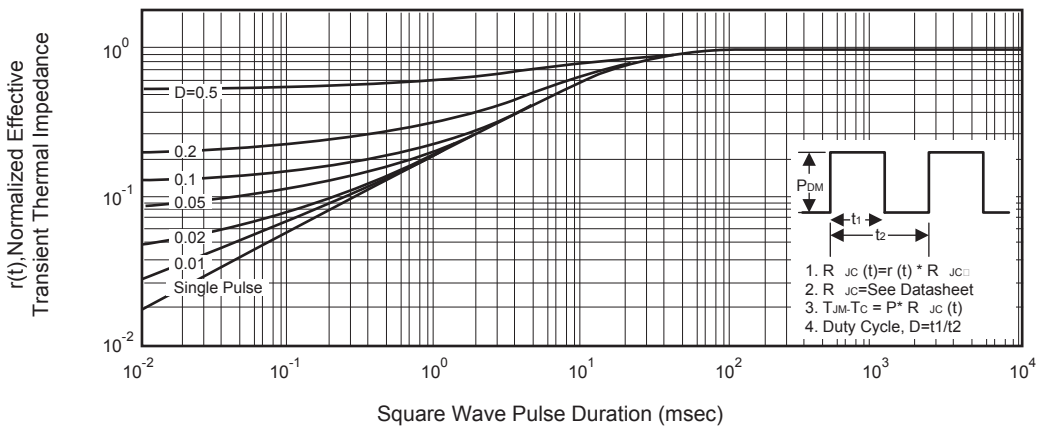


Figure 11. Normalized Thermal Transient Impedance Curve