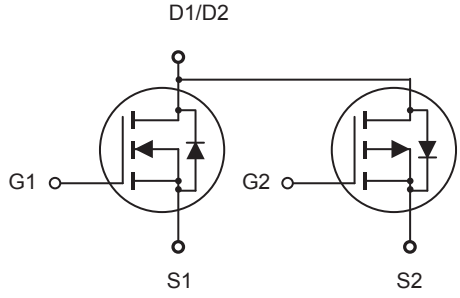
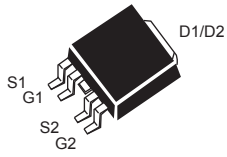
# CEU4269

## Dual Enhancement Mode Field Effect Transistor (N and P Channel)

## FEATURES

- 40V , 14A , $R_{DS(ON)}$ = 32mΩ @$V_{GS}$ = 10V.
  $R_{DS(ON)}$ = 46mΩ @$V_{GS}$ = 4.5V.
- -40V , -12A , $R_{DS(ON)}$ = 45mΩ @$V_{GS}$ = 10V.
  $R_{DS(ON)}$ = 65mΩ @$V_{GS}$ = 4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-252-4L package.




CEU SERIES
TO-252-4L

## ABSOLUTE MAXIMUM RATINGS $T_C$ = 25°C unless otherwise noted

| Parameter | Symbol | N-Channel | P-Channel | Units |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 40 | 40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | ±20 | V |
| Drain Current-Continuous [e] | $I_D$ [e] | 14 | -12 | A |
| Drain Current-Pulsed [a] | $I_{DM}$ | 56 | -48 | A |
| Maximum Power Dissipation @ $T_C$ = 25°C | $P_D$ | 10.4 | | W |
| - Derate above 25°C | | 0.08 | | W/°C |
| Operating and Store Temperature Range | $T_J$,$T_{stg}$ | -55 to 150 | | °C |

## Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 12 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 50 | °C/W |

## N-Channel Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40V, $V_{GS}$ = 0V | | | 1 | μA |
| Gate Body Leakage Current, Forward | $I_{GSSF}$ | $V_{GS}$ = 20V, $V_{DS}$ = 0V | | | 100 | nA |
| Gate Body Leakage Current, Reverse | $I_{GSSR}$ | $V_{GS}$ = -20V, $V_{DS}$ = 0V | | | -100 | nA |
| **On Characteristics** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1 | | 3 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 7A | | 25 | 32 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 5A | | 35 | 46 | mΩ |
| **Dynamic Characteristics** [d] | | | | | | |
| Forward Transconductance | $g_{FS}$ [c] | $V_{DS}$ = 10V, $I_D$ = 7A | | 3 | | S |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 20V, $V_{GS}$ = 0V, f = 1.0 MHz | | 1050 | | pF |
| Output Capacitance | $C_{oss}$ | | | 155 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 95 | | pF |
| **Switching Characteristics** [d] | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20V, $I_D$ = 6A, $V_{GS}$ = 10V, $R_{GEN}$ = 3Ω | | 14 | 30 | ns |
| Turn-On Rise Time | $t_r$ | | | 10 | 20 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 17 | 35 | ns |
| Turn-Off Fall Time | $t_f$ | | | 18 | 35 | ns |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 20V, $I_D$ = 6A, $V_{GS}$ = 10V | | 20.5 | 27 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 3.5 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 4.0 | | nC |
| **Drain-Source Diode Characteristics and Maximun Ratings** | | | | | | |
| Drain-Source Diode Forward Current [b] | $I_S$ | | | | 8 | A |
| Drain-Source Diode Forward Voltage [c] | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = 1.0A | | | 1.2 | V |

**Notes :**
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.
e.Calculated continuous current based on the maximum allowable junction temperature. Package limitation current=8A.

## P-Channel Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250μA | -40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -40V, $V_{GS}$ = 0V | | | -1 | μA |
| Gate Body Leakage Current, Forward | $I_{GSSF}$ | $V_{GS}$ = 20V, $V_{DS}$ = 0V | | | 100 | nA |
| Gate Body Leakage Current, Reverse | $I_{GSSR}$ | $V_{GS}$ = -20V, $V_{DS}$ = 0V | | | -100 | nA |
| **On Characteristics** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = -250μA | -1 | | -3 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$ = -10V, $I_D$ = -5A | | 37 | 45 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -3A | | 50 | 65 | mΩ |
| **Dynamic Characteristics** [d] | | | | | | |
| Forward Transconductance [c] | $g_{FS}$ | $V_{DS}$ = -10V, $I_D$ = -5A | | 3 | | S |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -20V, $V_{GS}$ = 0V, f = 1.0 MHz | | 1125 | | pF |
| Output Capacitance | $C_{oss}$ | | | 150 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 100 | | pF |
| **Switching Characteristics** [d] | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -20V, $I_D$ = -5A, $V_{GS}$ = -10V, $R_{GEN}$ = 3Ω | | 12 | 24 | ns |
| Turn-On Rise Time | $t_r$ | | | 5 | 10 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 33 | 66 | ns |
| Turn-On Fall Time | $t_f$ | | | 4 | 8 | ns |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -20V, $I_D$ = -5A, $V_{GS}$ = -10V | | 20 | 26 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 3 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 4 | | nC |
| **Drain-Source Diode Characteristics and Maximun Ratings** | | | | | | |
| Drain-Source Diode Forward Current [b] | $I_S$ | | | | -8 | A |
| Drain-Source Diode Forward Voltage [c] | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = -1.0A | | | -1.2 | V |

**Notes :**
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.
e.Calculated continuous current based on the maximum allowable junction temperature. Package limitation current=8A.

## N-CHANNEL

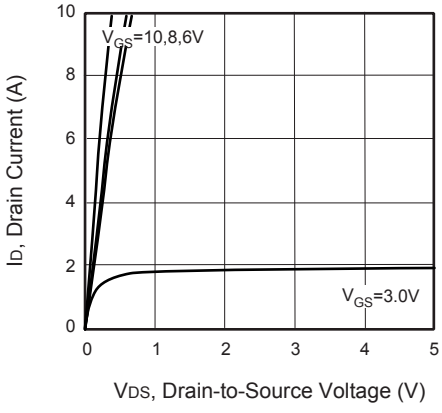



**Figure 1. Output Characteristics**

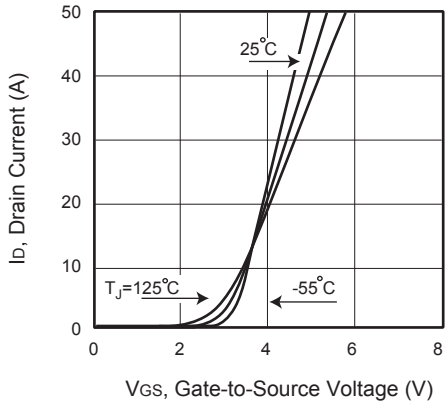



**Figure 2. Transfer Characteristics**

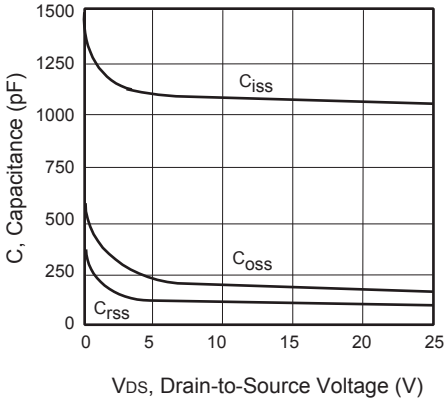



**Figure 3. Capacitance**

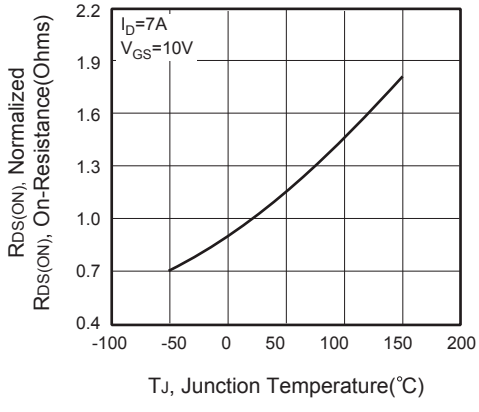



**Figure 4. On-Resistance Variation with Temperature**

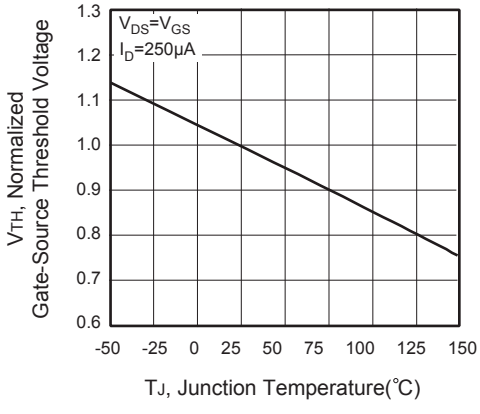



**Figure 5. Gate Threshold Variation with Temperature**

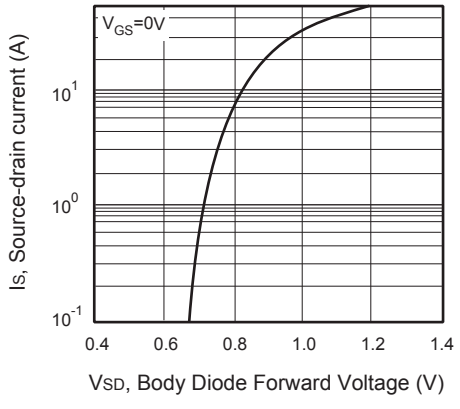



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

## P-CHANNEL

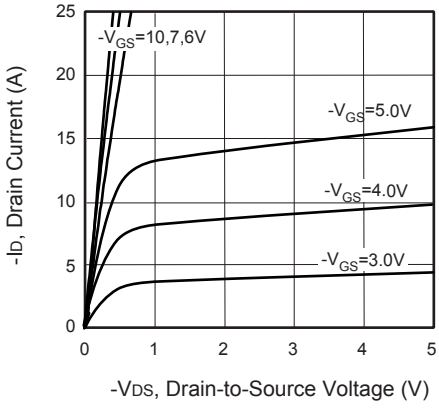



**Figure 7. Output Characteristics**

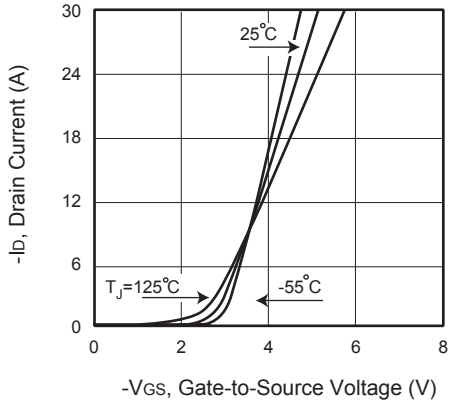



**Figure 8. Transfer Characteristics**

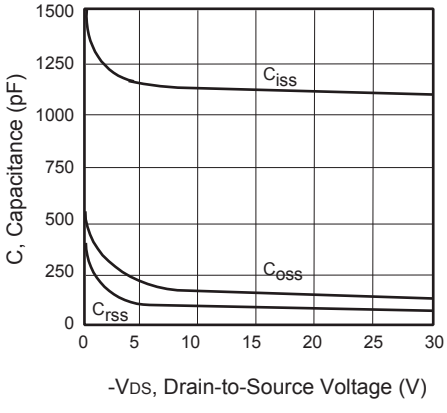



**Figure 9. Capacitance**

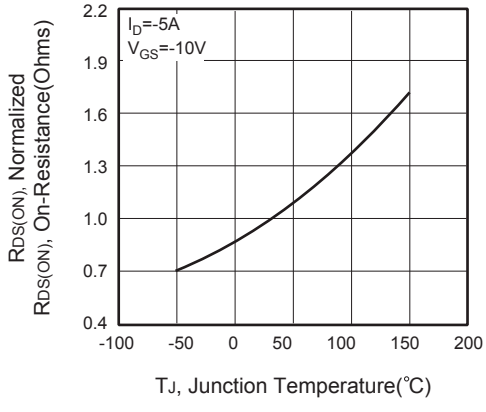



**Figure 10. On-Resistance Variation with Temperature**

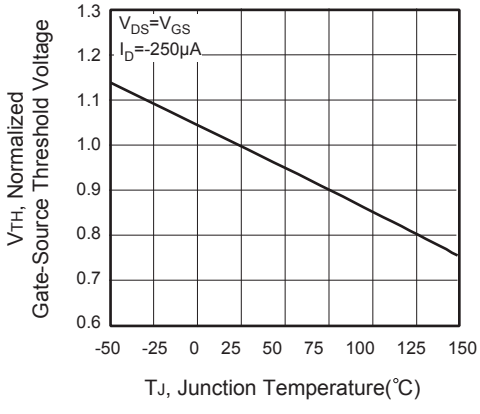



**Figure 11. Gate Threshold Variation with Temperature**

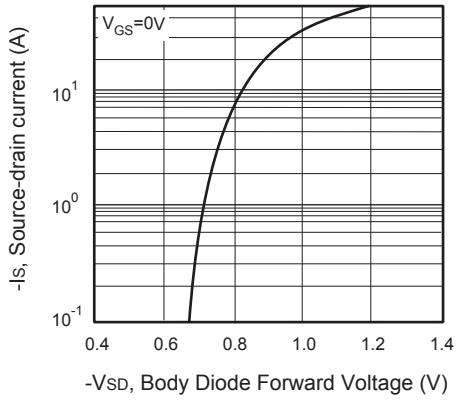



**Figure 12. Body Diode Forward Voltage Variation with Source Current**

## N-CHANNEL

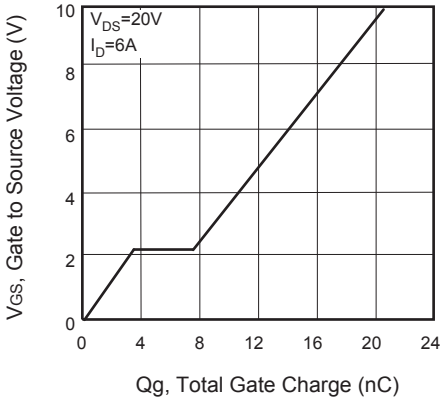



**Figure 13. Gate Charge**

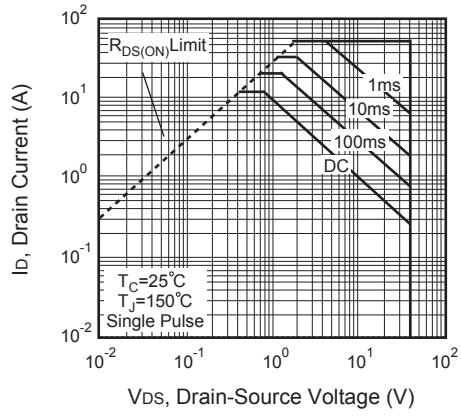



**Figure 14. Maximum Safe Operating Area**

## P-CHANNEL

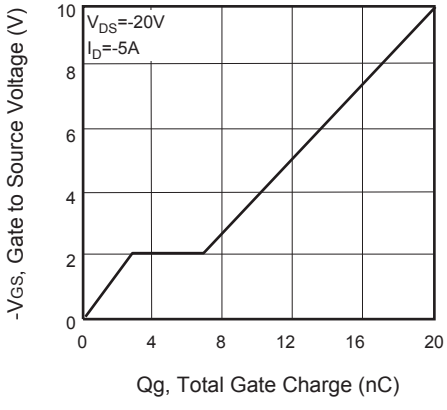



**Figure 15. Gate Charge**

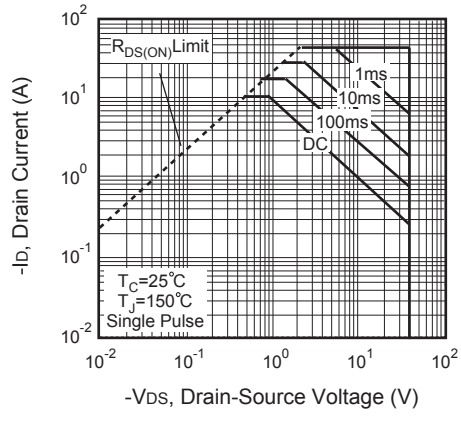



**Figure 16. Maximum Safe Operating Area**

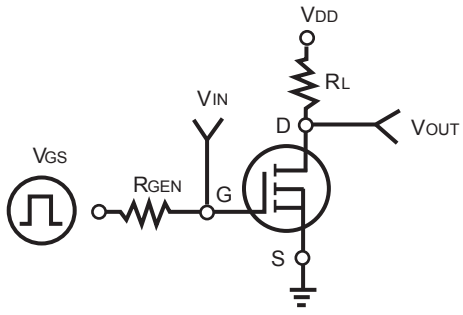



**Figure 17. Switching Test Circuit**

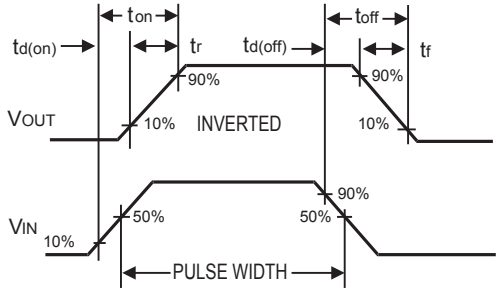



**Figure 18. Switching Waveforms**

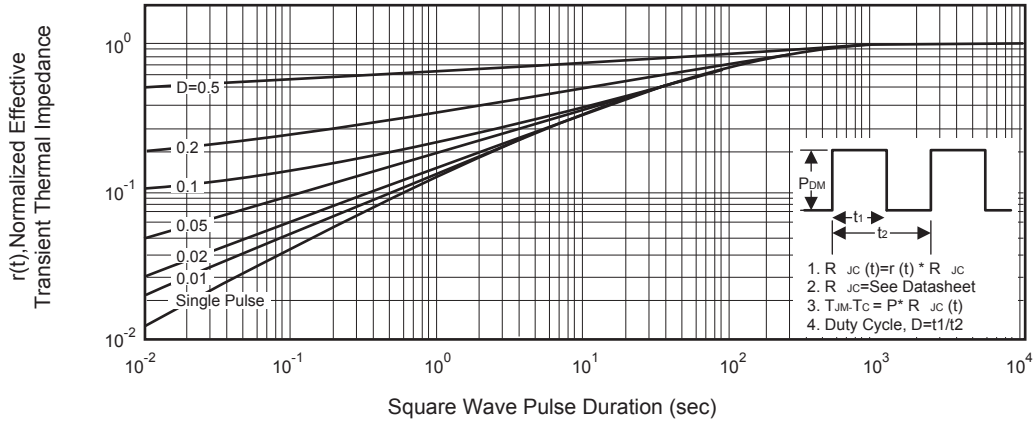



**Figure 19. Normalized Thermal Transient Impedance Curve**