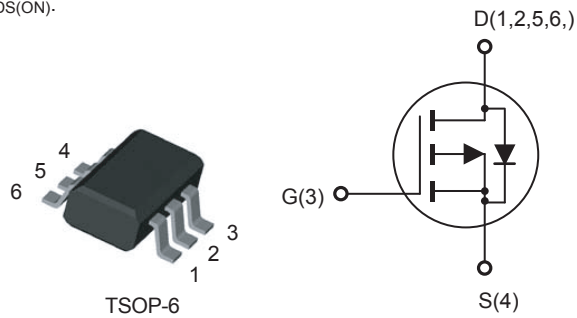


## P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

- -30V, -4.9A,  $R_{DS(ON)} = 52m\Omega$  @ $V_{GS} = -10V$ .
  - $R_{DS(ON)} = 65m\Omega$  @ $V_{GS} = -4.5V$ . □
  - $R_{DS(ON)} = 119m\Omega$  @ $V_{GS} = -2.5V$ . □
- High dense cell design for extremely low  $R_{DS(ON)}$ .
- Rugged and reliable.
- Lead free product is acquired.
- TSOP-6 package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

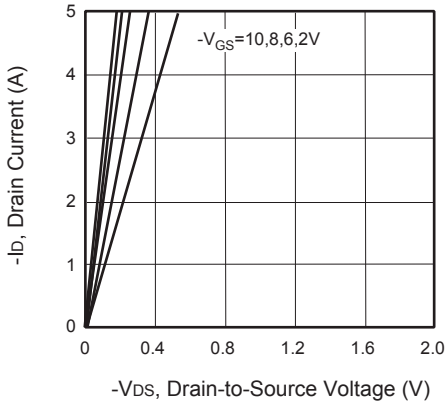
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	-4.9	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	-20	A
Maximum Power Dissipation	$P_D$	2.0	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

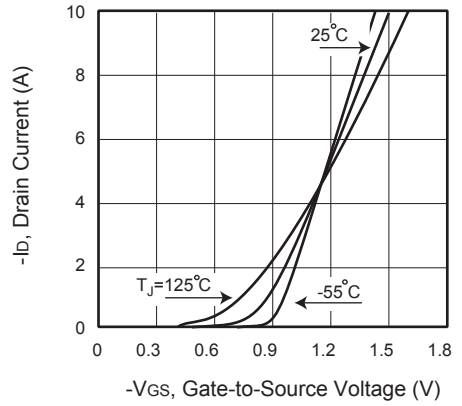
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

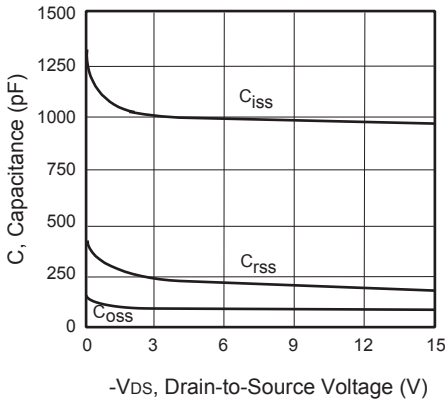
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 12V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -12V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-0.7		-1.3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.9A$		42	52	$m\Omega$
		$V_{GS} = -4.5V, I_D = -2.2A$		54	65	$m\Omega$
		$V_{GS} = -2.5V, I_D = -1.2A$		82	119	$m\Omega$
<b>Dynamic Characteristics <sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		945		pF
Output Capacitance	$C_{oss}$			120		pF
Reverse Transfer Capacitance	$C_{rss}$			80		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -4.0A, \square$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		9		ns
Turn-On Rise Time	$t_r$			3		ns
Turn-Off Delay Time	$t_{d(off)}$			66		ns
Turn-Off Fall Time	$t_f$			16		ns
Total Gate Charge	$Q_g$	$V_{DS} = -15V, I_D = -4.0A,$ $V_{GS} = -4.5V$		9		nC
Gate-Source Charge	$Q_{gs}$			1		nC
Gate-Drain Charge	$Q_{gd}$			3		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-4.9	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -1A$			-1	V
<b>Notes :</b> <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature. <input type="checkbox"/> b.Surface Mounted on FR4 Board, $t < 5 \text{ sec.}$ <input type="checkbox"/> c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . <input type="checkbox"/> d.Guaranteed by design, not subject to production testing. <input type="checkbox"/> <input type="checkbox"/>						



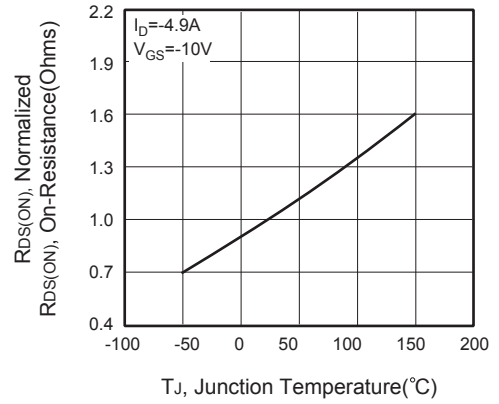
**Figure 1. Output Characteristics**



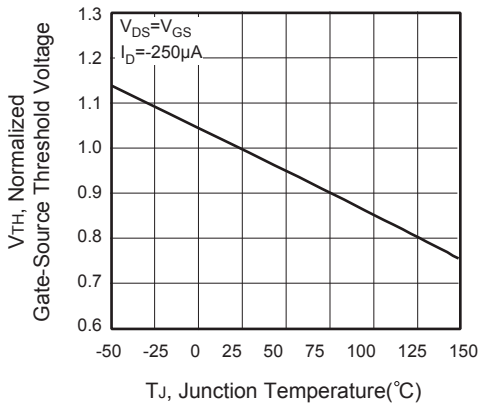
**Figure 2. Transfer Characteristics**



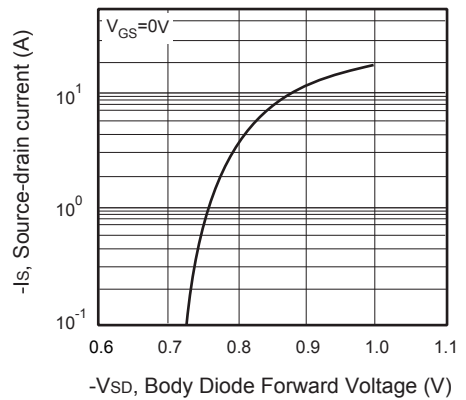
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

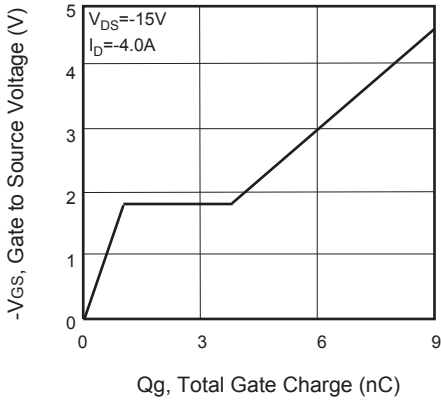


Figure 7. Gate Charge

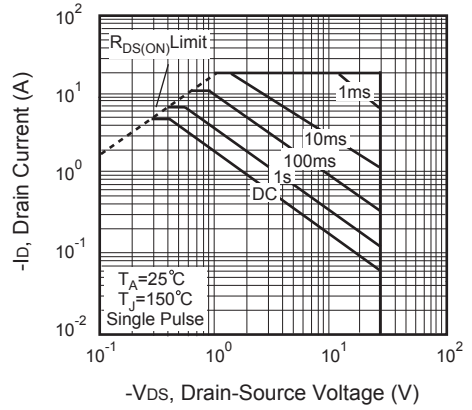


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit

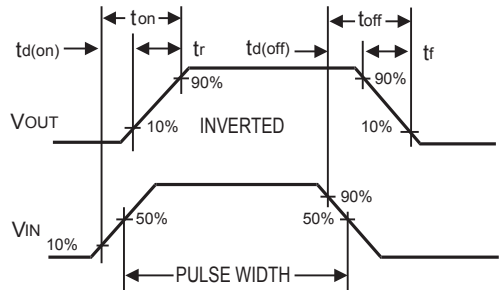


Figure 10. Switching Waveforms

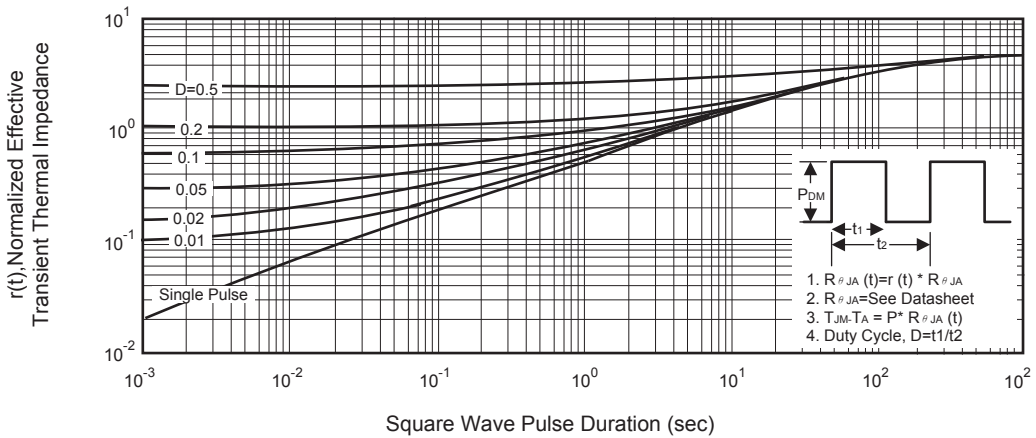


Figure 11. Normalized Thermal Transient Impedance Curve