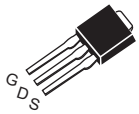
CED40N20/CEU40N20

N-Channel Enhancement Mode Field Effect Transistor

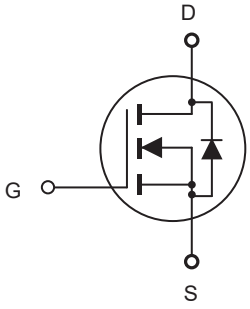
FEATURES

- 200V, 40A, $R_{DS(ON)}$ = 32mΩ @V_{GS} = 10V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant
- TO-251 & TO-252 package.

CEU SERIES
TO-252(D-PAK)



CED SERIES
TO-251(I-PAK)



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous @ T_C = 25°C	I_D	40	A
@ T_C = 100°C		28	A
Drain Current-Pulsed [a]	I_{DM}	160	A
Maximum Power Dissipation @ T_C = 25°C	P_D	107	W
- Derate above 25°C		0.71	W/°C
Single Pulsed Avalanche Energy [d]	E_{AS}	180	mJ
Single Pulsed Avalanche Current [d]	I_{AS}	30	A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 10A		27	32	mΩ
Gate input resistance	R_g	f=1MHz,open Drain		4.5		Ω
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 100V, V_{GS}=0V, f = 1.0 MHz		1470		pF
Output Capacitance	C_{oss}			170		pF
Reverse Transfer Capacitance	C_{rss}			10		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100V, I_D = 10A, V_{GS} = 10V, R_{GEN} = 10Ω		27		ns
Turn-On Rise Time	t_r			12		ns
Turn-Off Delay Time	$t_{d(off)}$			44		ns
Turn-Off Fall Time	t_f			16		ns
Total Gate Charge	Q_g	V_{DS} = 100V, I_D = 10A, V_{GS} = 10V		22		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				40	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 10A			1.2	V
Reverse Recovery Time	T_{rr}	I_F = 10A, dI_F /dt = 100A/us		93		ns
Reverse Recovery Charge	Q_{rr}			305		nC

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.
d.L = 0.4mH, I_{AS} = 30A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.

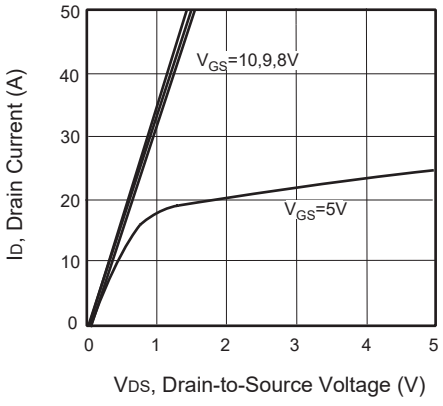


Figure 1. Output Characteristics

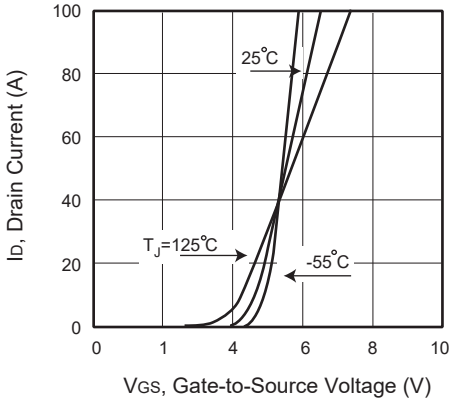


Figure 2. Transfer Characteristics

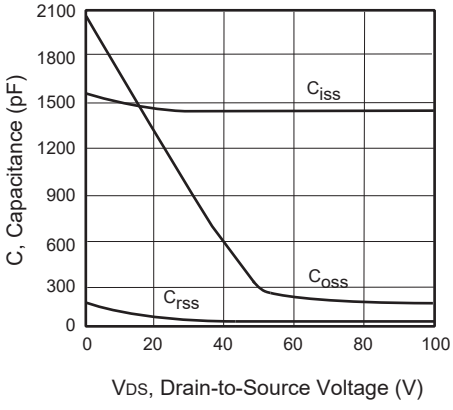


Figure 3. Capacitance

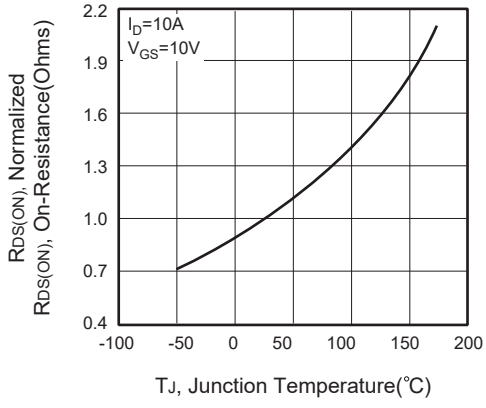


Figure 4. On-Resistance Variation with Temperature

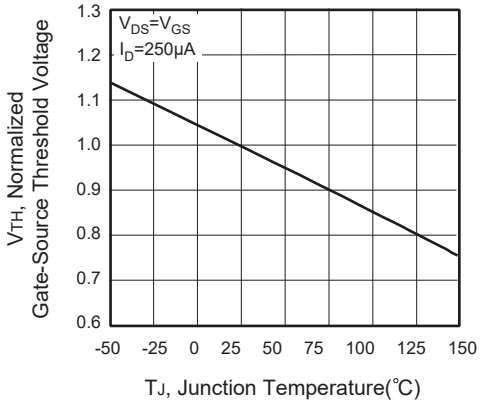


Figure 5. Gate Threshold Variation with Temperature

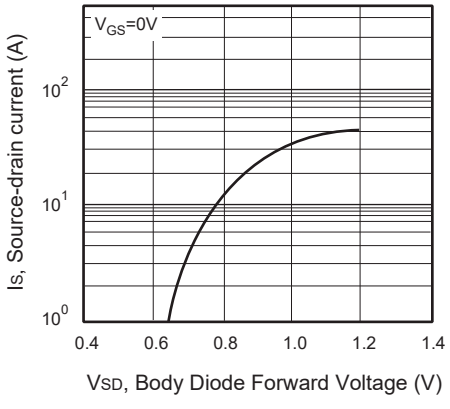


Figure 6. Body Diode Forward Voltage Variation with Source Current

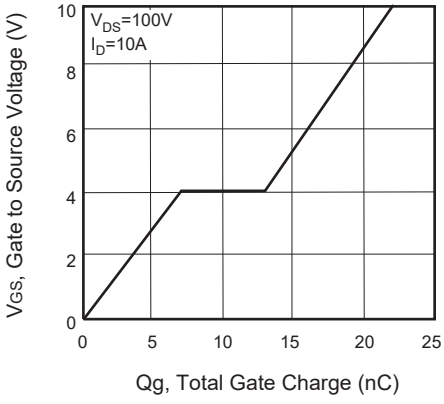


Figure 7. Gate Charge

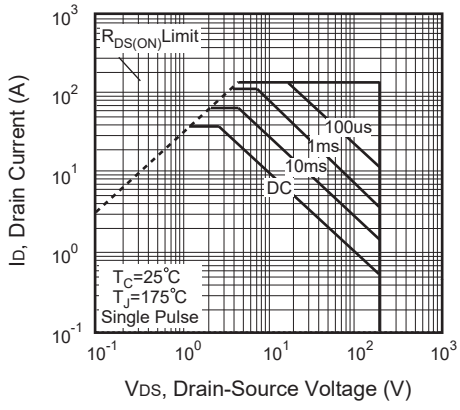


Figure 8. Maximum Safe Operating Area

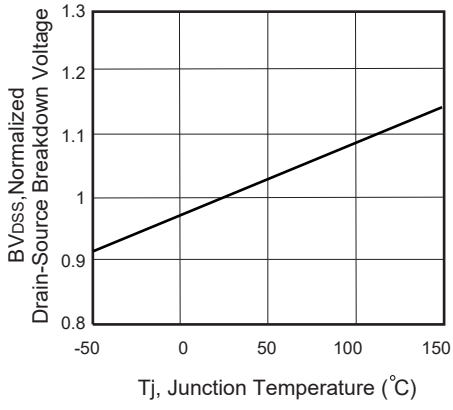


Figure 9. Breakdown Voltage Variation VS Temperature

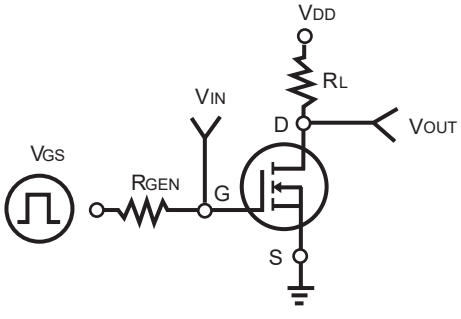


Figure 10. Switching Test Circuit

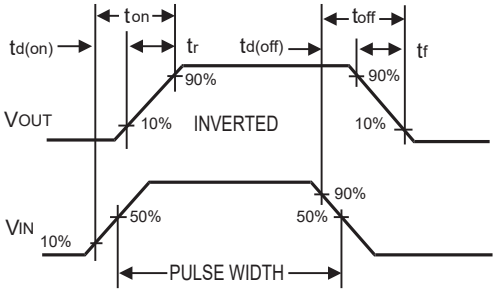


Figure 11. Switching Waveforms

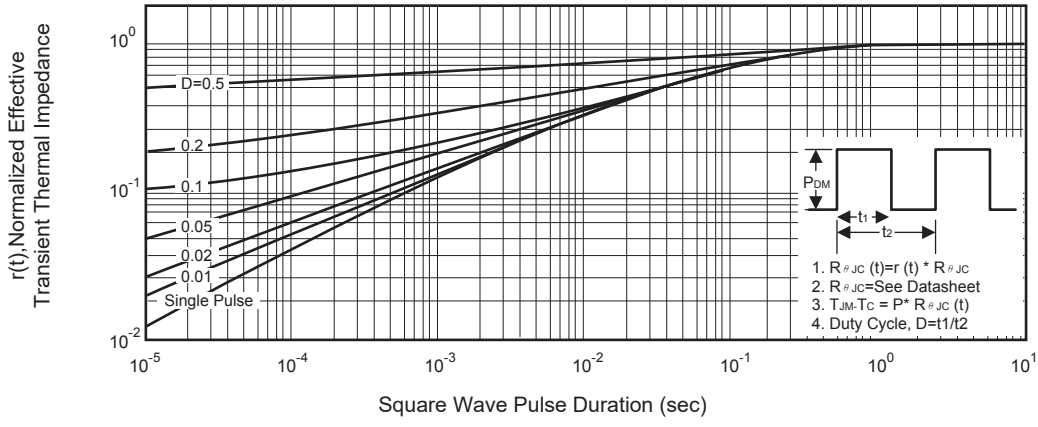


Figure 12. Normalized Thermal Transient Impedance Curve