

## N-Channel Enhancement Mode Field Effect Transistor

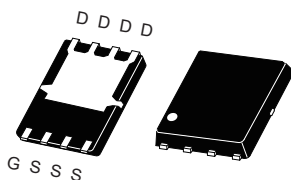
PRELIMINARY

### FEATURES

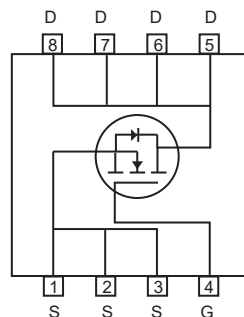
- 65V, 199A,  $R_{DS(ON)} = 1.35m\Omega$  @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.

### APPLICATIONS

- Synchronous rectification.
- DC/DC converter.
- Motor drive switch.
- Battery and load switch.



P-PAK 5X6



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

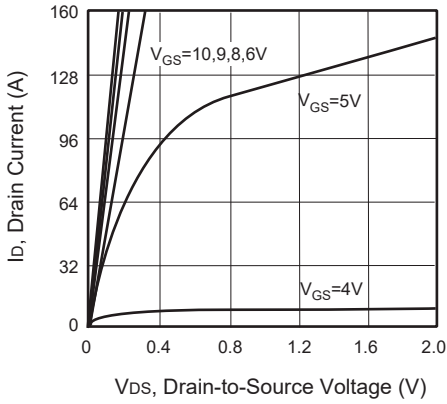
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	65	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	199	A
	$I_D @ R_{\theta JA}$	51	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{\theta JC}$	796	A
	$I_{DM} @ R_{\theta JA}$	204	A
Maximum Power Dissipation	$P_D$	96	W
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	1058	mJ
Repetitive Avalanche Energy <sup>d</sup>	$E_{AR}$	9.6	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	46	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

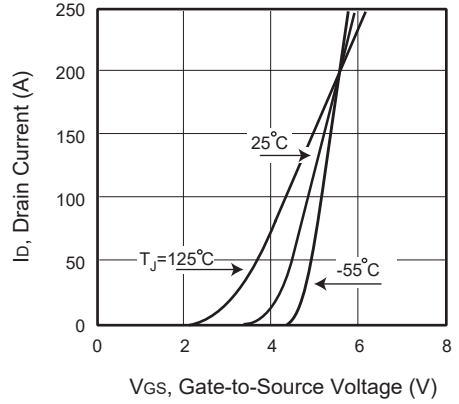
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.3	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	20	$^\circ C/W$

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

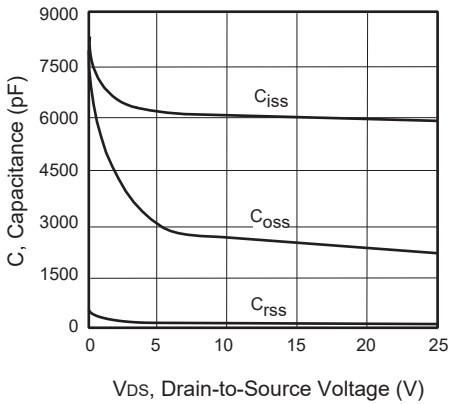
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	65			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 65V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		1.05	1.35	m $\Omega$
Gate Input Resistance	$R_g$	f=1MHz, open Drain		2.8		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		5980		pF
Output Capacitance	$C_{oss}$			2335		pF
Reverse Transfer Capacitance	$C_{rss}$			80		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V, I_D = 20A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		40		ns
Turn-On Rise Time	$t_r$			36		ns
Turn-Off Delay Time	$t_{d(off)}$			86		ns
Turn-Off Fall Time	$t_f$			58		ns
Total Gate Charge	$Q_g$	$V_{DS} = 30V, I_D = 20A,$ $V_{GS} = 10V$		97		nC
Gate-Source Charge	$Q_{gs}$			19		nC
Gate-Drain Charge	$Q_{gd}$			40		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				80	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 20A$			1.2	V
Reverse Recovery Time	$T_{rr}$	$I_F = 20A, di/dt = 100A/\mu s$		96		ns
Reverse Recovery Charge	$Q_{rr}$			228		nC
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.L = 1mH, $I_{AS} = 46A, V_{DD} = 24V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ .						



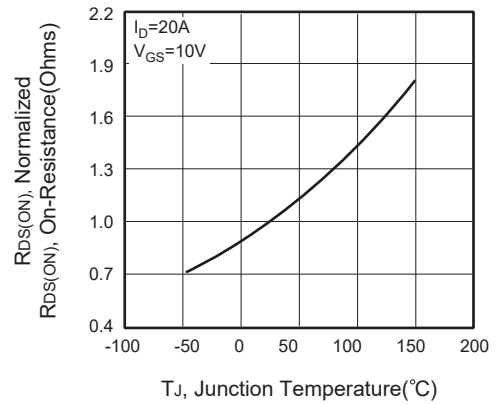
**Figure 1. Output Characteristics**



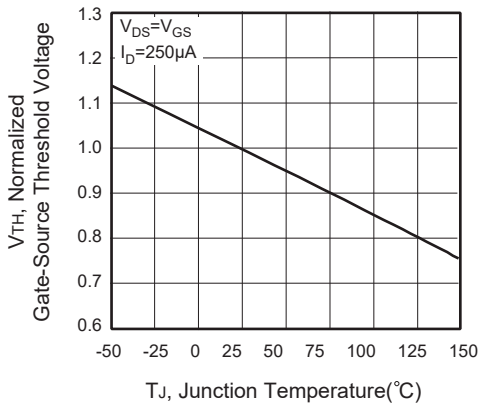
**Figure 2. Transfer Characteristics**



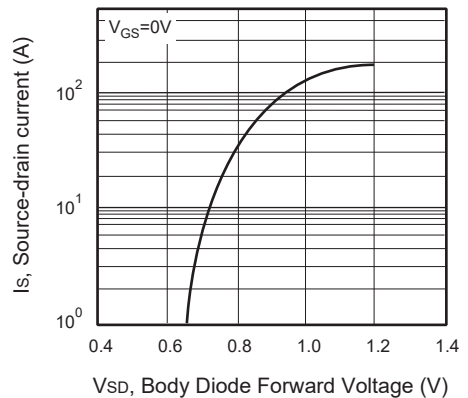
**Figure 3. Capacitance**



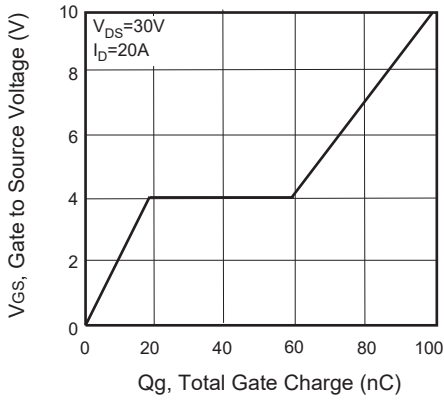
**Figure 4. On-Resistance Variation with Temperature**



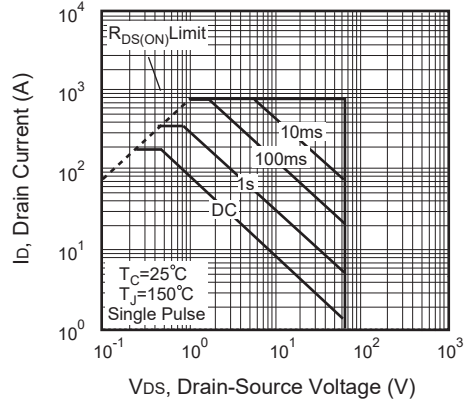
**Figure 5. Gate Threshold Variation with Temperature**



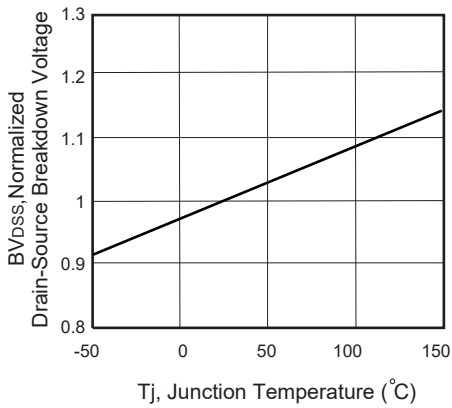
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



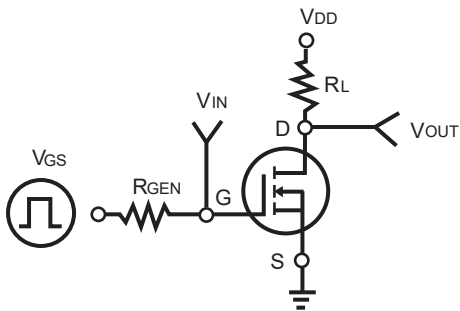
**Figure 7. Gate Charge**



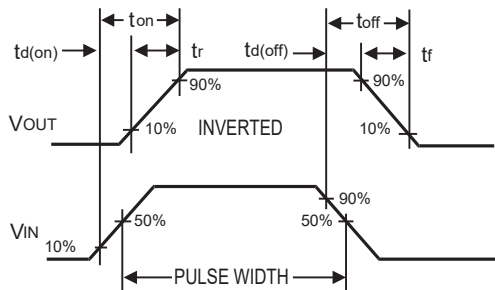
**Figure 8. Maximum Safe Operating Area**



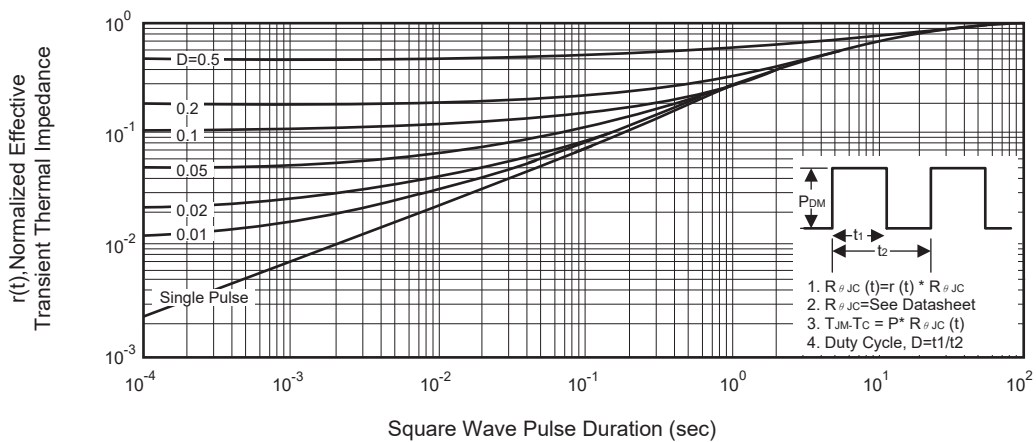
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



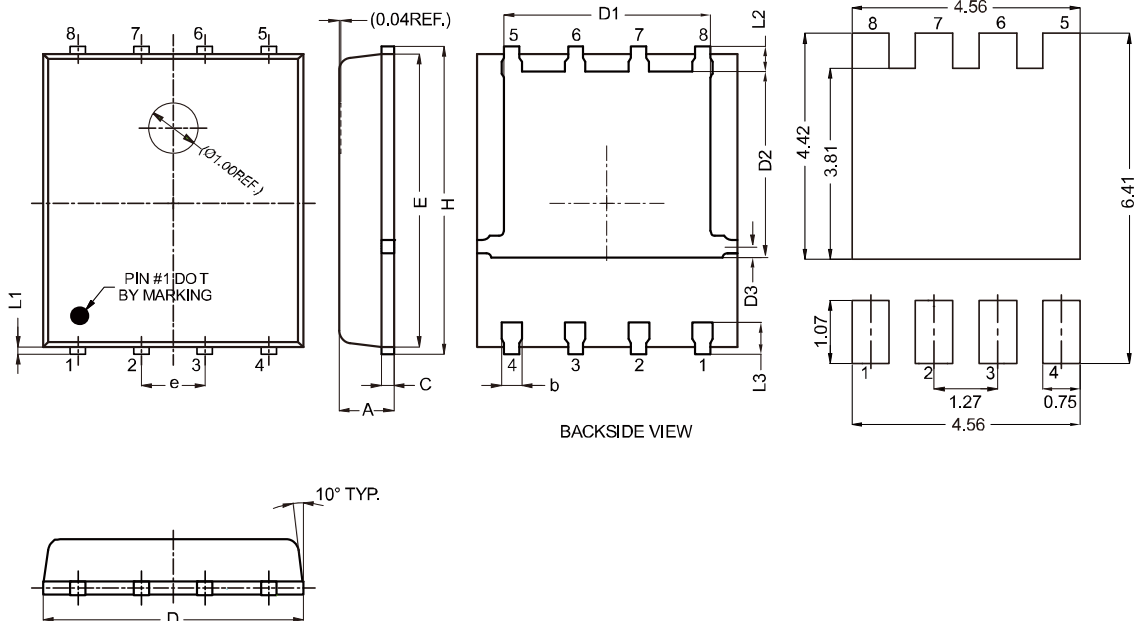
**Figure 11. Switching Waveforms**



**Figure 12. Normalized Thermal Transient Impedance Curve**

## P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

### SINGLE PAD 尺寸圖



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.200	0.031	0.047
b	0.200	0.510	0.008	0.020
c	0.150	0.350	0.006	0.014
D	4.800	5.400	0.189	0.213
D1	3.610	4.400	0.142	0.173
D2	3.300	4.300	0.130	0.169
D3	0.396	0.600	0.016	0.024
E	5.400	6.100	0.213	0.240
e	1.270 TYP		0.050 TYP	
H	5.850	6.300	0.230	0.248
L1	0.080	0.330	0.003	0.013
L2	0.400	0.800	0.016	0.031
L3	0.460	0.740	0.018	0.029