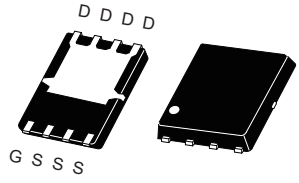
CEZ25R4

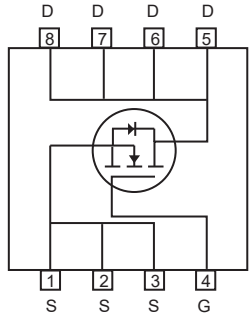
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 40V, 113A, $R_{DS(ON)}$ = 3.2mΩ @V_{GS} = 10V.
  $R_{DS(ON)}$ = 4.8mΩ @V_{GS} = 4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.
- Surface mount Package.



P-PAK 5X6



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D @$R_{\theta JA}$	34	A
Drain Current-Continuous	I_D @$R_{\theta JC}$	113	A
Drain Current-Pulsed [a]	I_{DM}@$R_{\theta JA}$	136	A
Drain Current-Pulsed [a]	I_{DM} @$R_{\theta JC}$	452	A
Maximum Power Dissipation	P_D	65	W
Single Pulsed Avalanche Energy [e]	E_{AS}	288	mJ
Single Pulsed Avalanche Current [e]	I_{AS}	24	A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.9	°C/W
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	20	°C/W

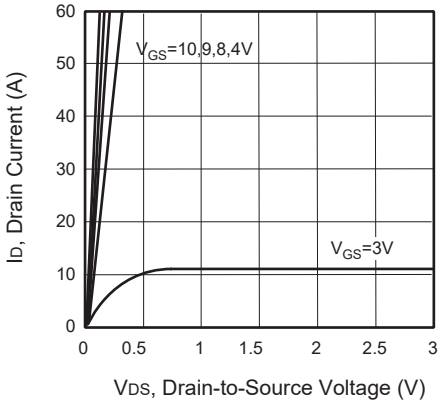


Figure 1. Output Characteristics

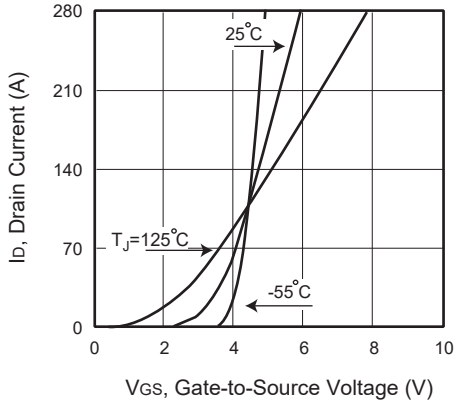


Figure 2. Transfer Characteristics

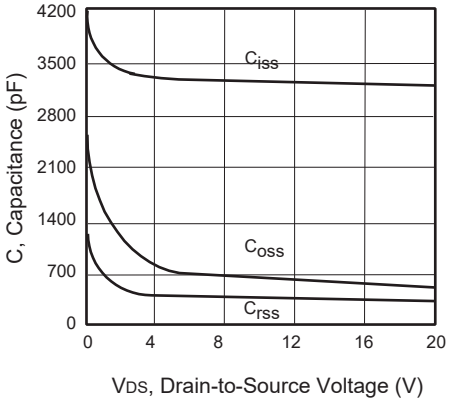


Figure 3. Capacitance

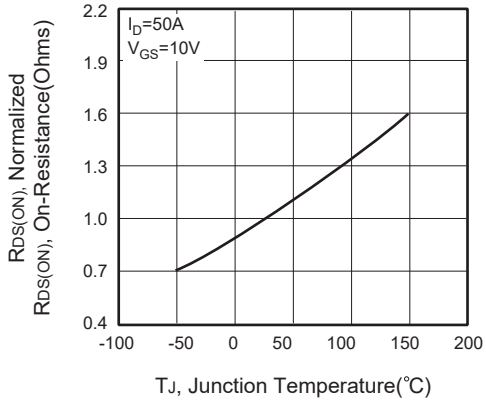


Figure 4. On-Resistance Variation with Temperature

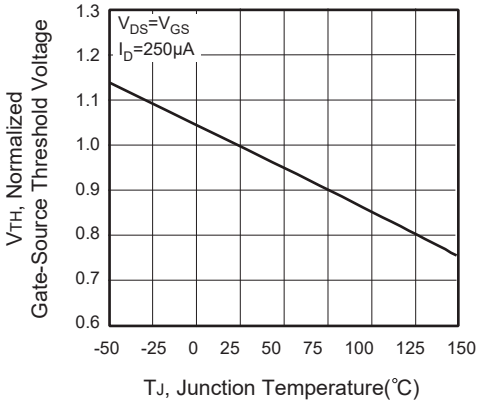


Figure 5. Gate Threshold Variation with Temperature

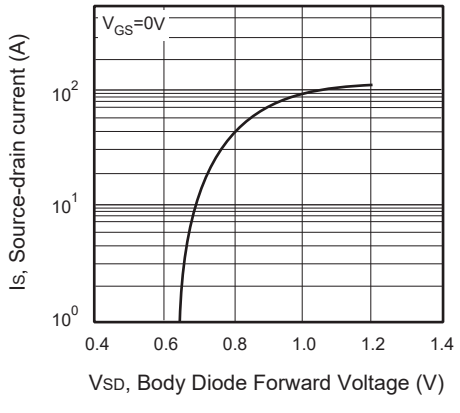


Figure 6. Body Diode Forward Voltage Variation with Source Current

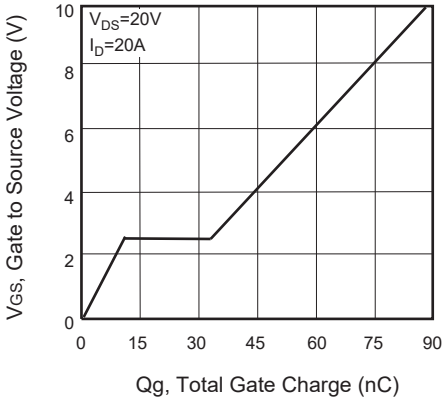


Figure 7. Gate Charge

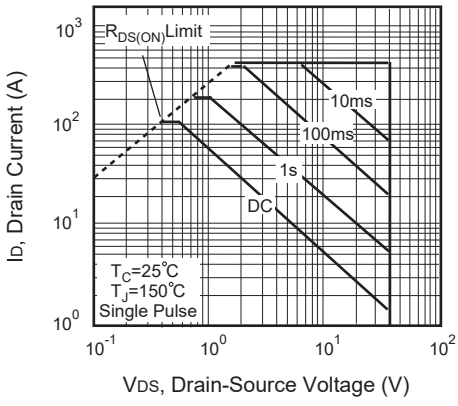


Figure 8. Maximum Safe Operating Area

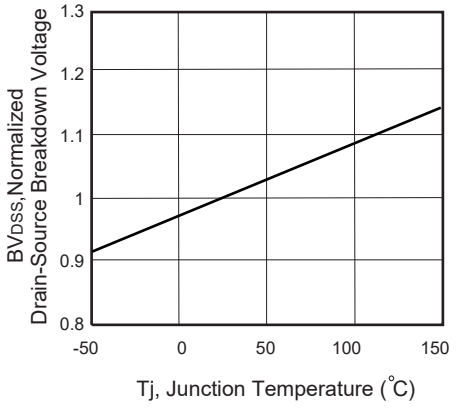


Figure 9. Breakdown Voltage Variation VS Temperature

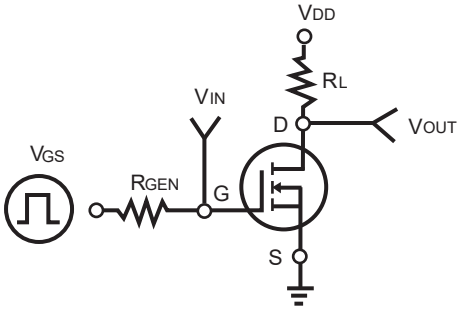


Figure 10. Switching Test Circuit

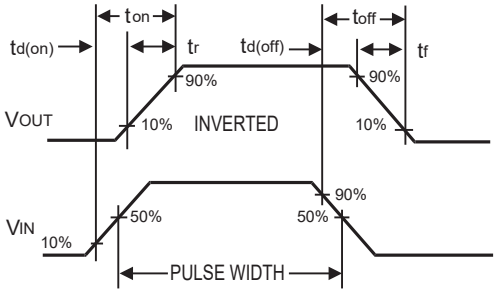


Figure 11. Switching Waveforms

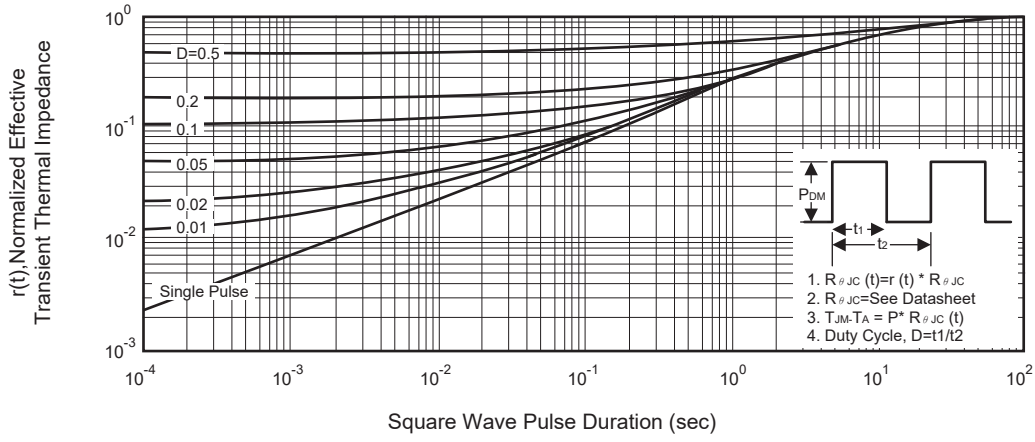


Figure 12. Normalized Thermal Transient Impedance Curve