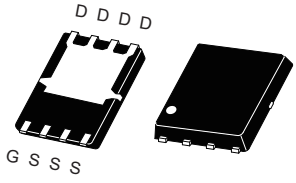
# CEZ3112

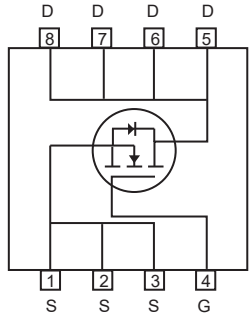
## N-Channel Enhancement Mode Field Effect Transistor

## FEATURES

- 30V, 43A, $R_{DS\ (ON)}$= 10.5 mΩ @$V_{GS}$ = 10V.
  $R_{DS\ (ON)}$= 15 mΩ @$V_{GS}$ = 4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.




P-PAK 5X6




## ABSOLUTE MAXIMUM RATINGS $T_C$ = 25°C unless otherwise noted

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ @$R_{\theta JC}$ | 43 | A |
| | $I_D$ @$R_{\theta JA}$ | 18 | A |
| Drain Current-Pulsed [a] | $I_{DM}$@$R_{\theta JC}$ | 172 | A |
| | $I_{DM}$ @$R_{\theta JA}$ | 72 | A |
| Maximum Power Dissipation | $P_D$ | 34.7 | W |
| Single Pulsed Avalanche Energy [d] | $E_{AS}$ | 50 | mJ |
| Single Pulsed Avalanche Current [d] | $I_{AS}$ | 10 | A |
| Operating and Store Temperature Range | $T_J$,$T_{stg}$ | -55 to 150 | °C |

## Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 3.6 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 20 | °C/W |

## Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30V, $V_{GS}$ = 0V | | | 1 | μA |
| Gate Body Leakage Current, Forward | $I_{GSSF}$ | $V_{GS}$ = 20V, $V_{DS}$ = 0V | | | 100 | nA |
| Gate Body Leakage Current, Reverse | $I_{GSSR}$ | $V_{GS}$ = -20V, $V_{DS}$ = 0V | | | -100 | nA |
| **On Characteristics** [b] | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1 | | 3 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 6A | | 8.7 | 10.5 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 3A | | 11.3 | 15 | mΩ |
| **Dynamic Characteristics** [c] | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 15V, $V_{GS}$ = 0V, f = 1.0 MHz | | 735 | | pF |
| Output Capacitance | $C_{oss}$ | | | 145 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 110 | | pF |
| **Switching Characteristics** [c] | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15V, $I_D$ = 10A, $V_{GS}$ = 10V, $R_{GEN}$ = 3Ω | | 13 | | ns |
| Turn-On Rise Time | $t_r$ | | | 7 | | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 45 | | ns |
| Turn-Off Fall Time | $t_f$ | | | 18 | | ns |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15V, $I_D$ = 10A, $V_{GS}$ = 4.5V | | 9.3 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.8 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 4.8 | | nC |
| **Drain-Source Diode Characteristics and Maximun Ratings** | | | | | | |
| Drain-Source Diode Forward Current | $I_S$ | | | | 34 | A |
| Drain-Source Diode Forward Voltage [b] | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = 1A | | | 1 | V |

**Notes :**
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.
d.L = 1mH, $I_{AS}$ = 10A, $V_{DD}$ = 25V, $R_G$ = 25Ω, Starting $T_J$ = 25°C.

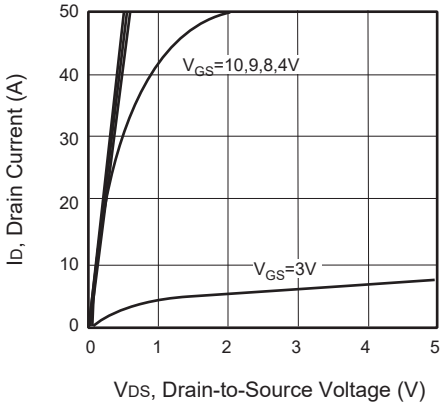



**Figure 1. Output Characteristics**

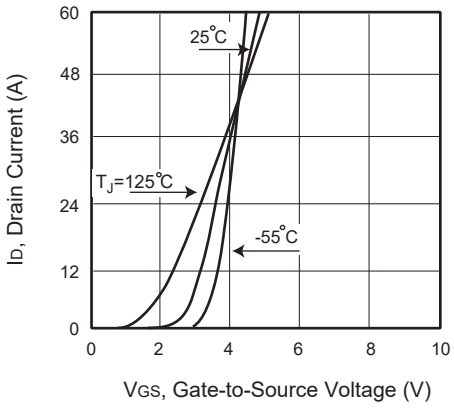



**Figure 2. Transfer Characteristics**

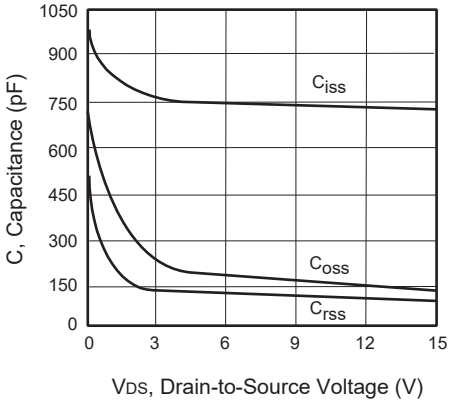



**Figure 3. Capacitance**

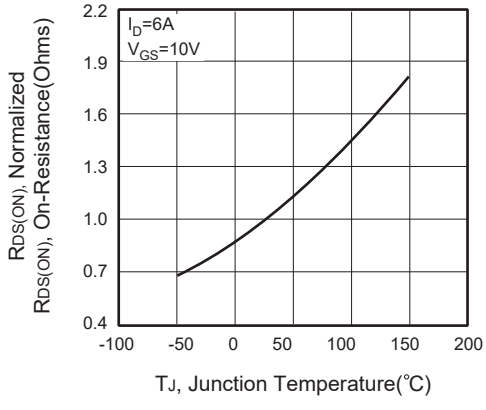



**Figure 4. On-Resistance Variation with Temperature**

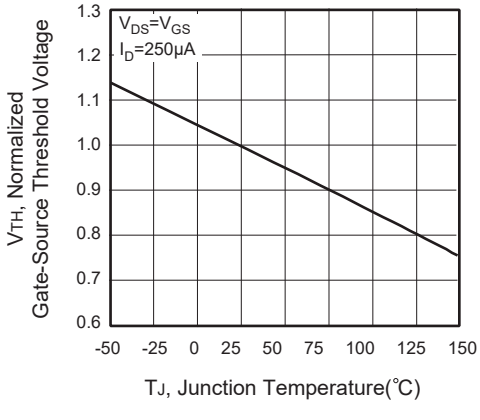



**Figure 5. Gate Threshold Variation with Temperature**

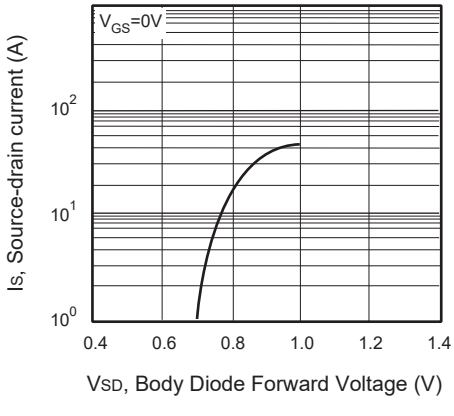



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

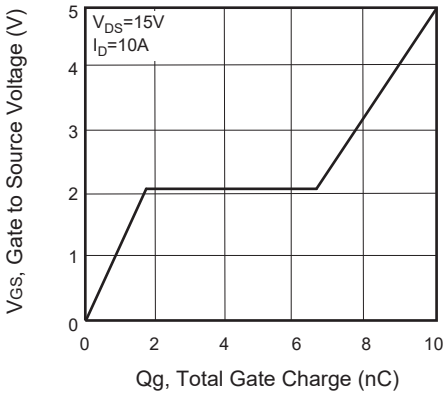



**Figure 7. Gate Charge**

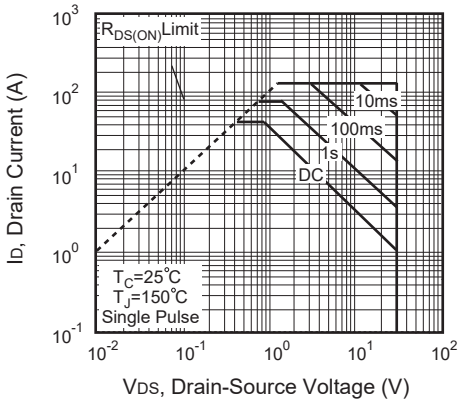



**Figure 8. Maximum Safe Operating Area**

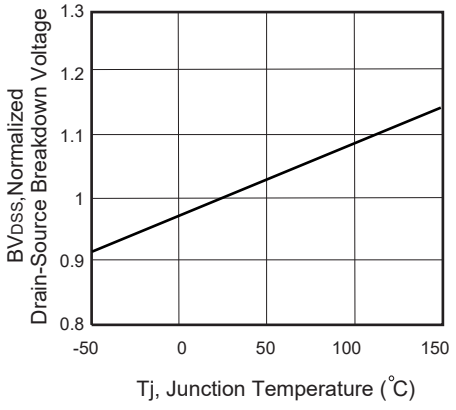



**Figure 9. Breakdown Voltage Variation VS Temperature**

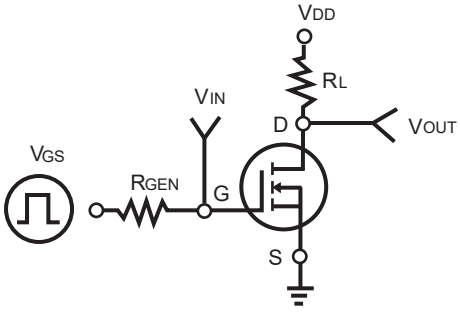



**Figure 10. Switching Test Circuit**

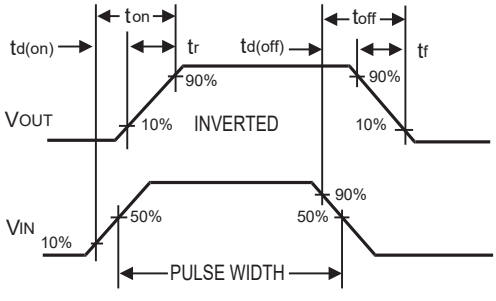



**Figure 11. Switching Waveforms**

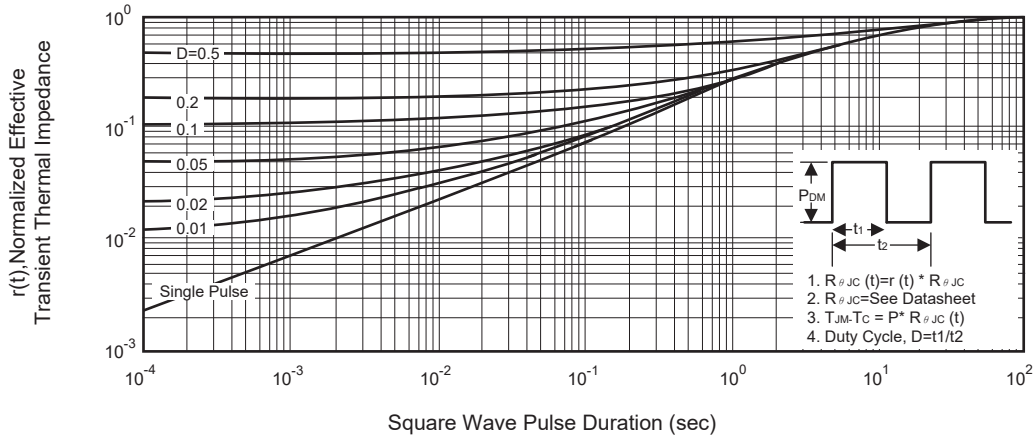
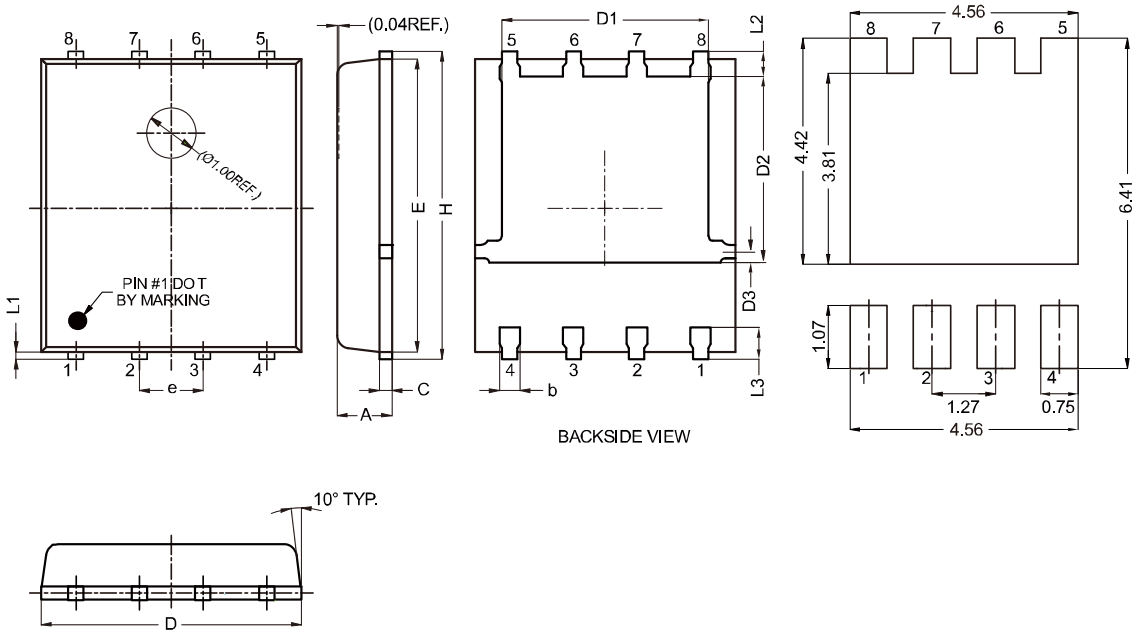



**Figure 12. Normalized Thermal Transient Impedance Curve**

## P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

**SINGLE PAD** 尺寸圖




| SYMBOLS | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 1.200 | 0.031 | 0.047 |
| b | 0.200 | 0.510 | 0.008 | 0.020 |
| c | 0.150 | 0.350 | 0.006 | 0.014 |
| D | 4.800 | 5.400 | 0.189 | 0.213 |
| D1 | 3.610 | 4.400 | 0.142 | 0.173 |
| D2 | 3.300 | 4.300 | 0.130 | 0.169 |
| D3 | 0.396 | 0.600 | 0.016 | 0.024 |
| E | 5.400 | 6.100 | 0.213 | 0.240 |
| e | 1.270 TYP | | 0.050 TYP | |
| H | 5.850 | 6.300 | 0.230 | 0.248 |
| L1 | 0.080 | 0.330 | 0.003 | 0.013 |
| L2 | 0.400 | 0.800 | 0.016 | 0.031 |
| L3 | 0.460 | 0.740 | 0.018 | 0.029 |