CEM4269B

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

■ 40V, 6.0A, $R_{DS(ON)}$ = 34mΩ @V_{GS} = 10V.
$R_{DS(ON)}$ = 49mΩ @V_{GS} = 4.5V.

■ -40V, -5.9A, $R_{DS(ON)}$ = 36mΩ @V_{GS} = -10V.
$R_{DS(ON)}$ = 44mΩ @V_{GS} = -4.5V.

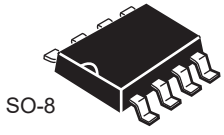
■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

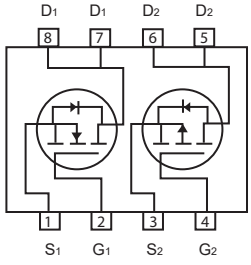
■ Pb-free lead plating ; RoHS compliant.

■ Halogen Free.

■ Surface mount Package.



1



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D	6	-5.9	A
Drain Current-Pulsed [a]	I_{DM}	24	-23.6	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics [a] T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6A		28	34	mΩ
		V_{GS} = 4.5V, I_D = 5A		38	49	mΩ
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		480		pF
Output Capacitance	C_{oss}			80		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 32V, R_L = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		9		ns
Turn-On Rise Time	t_r			4		ns
Turn-Off Delay Time	$t_{d(off)}$			28		ns
Turn-Off Fall Time	t_f			4		ns
Total Gate Charge	Q_g	V_{DS} = 32V, I_D = 1A, V_{GS} = 4.5V		5.7		nC
Gate-Source Charge	Q_{gs}			0.9		nC
Gate-Drain Charge	Q_{gd}			2.8		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				2	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 1A			1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics [a] $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -3A		30	36	mΩ
		V_{GS} = -4.5V, I_D = -2A		34	44	mΩ
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = -20V, V_{GS} = 0V, f = 1.0 MHz		1520		pF
Output Capacitance	C_{oss}			120		pF
Reverse Transfer Capacitance	C_{rss}			85		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -20V, I_D = -5A, V_{GS} = -10V, R_{GEN} = 3Ω		13		ns
Turn-On Rise Time	t_r			5		ns
Turn-Off Delay Time	$t_{d(off)}$			90		ns
Turn-Off Fall Time	t_f			16		ns
Total Gate Charge	Q_g	V_{DS} = -20V, I_D = -5A, V_{GS} = -4.5V		11		nC
Gate-Source Charge	Q_{gs}			3.2		nC
Gate-Drain Charge	Q_{gd}			4.4		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				-2	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

N-CHANNEL

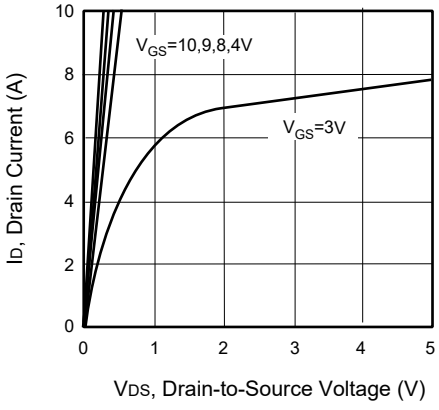


Figure 1. Output Characteristics

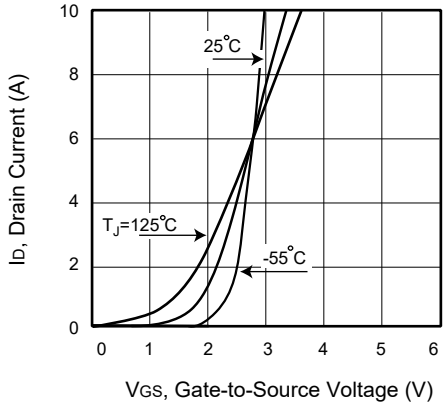


Figure 2. Transfer Characteristics

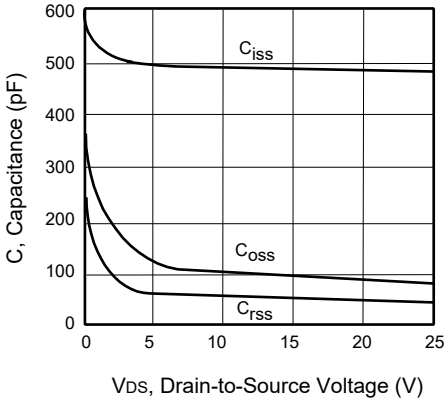


Figure 3. Capacitance

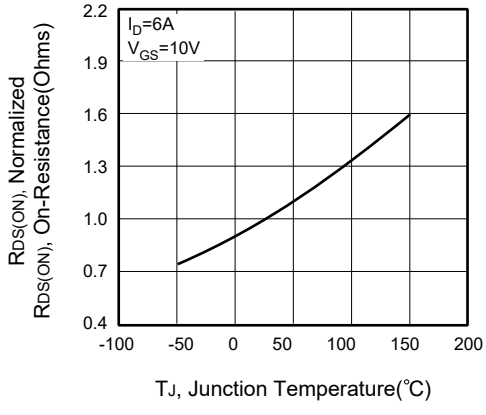


Figure 4. On-Resistance Variation with Temperature

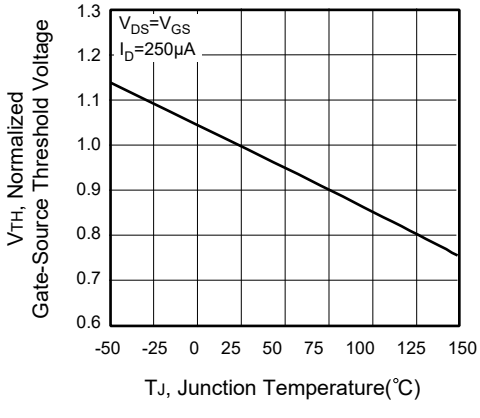


Figure 5. Gate Threshold Variation with Temperature

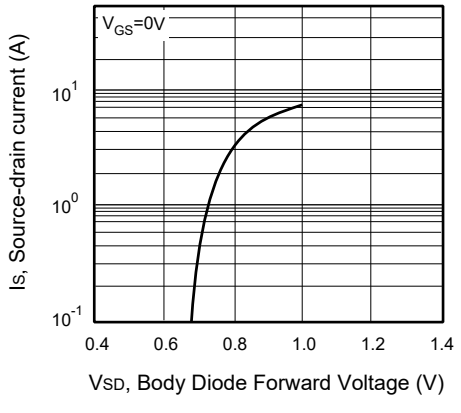


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

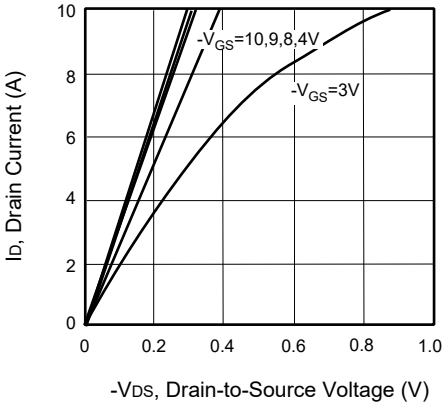


Figure 7. Output Characteristics

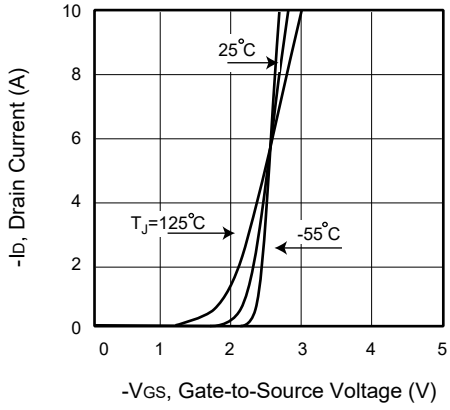


Figure 8. Transfer Characteristics

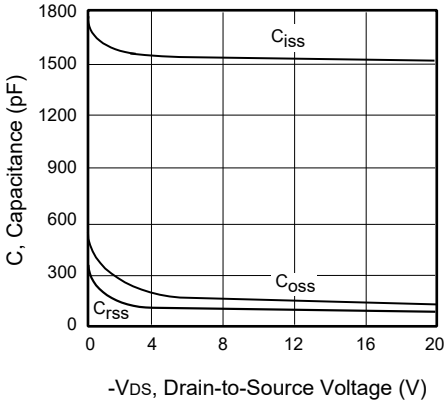


Figure 9. Capacitance

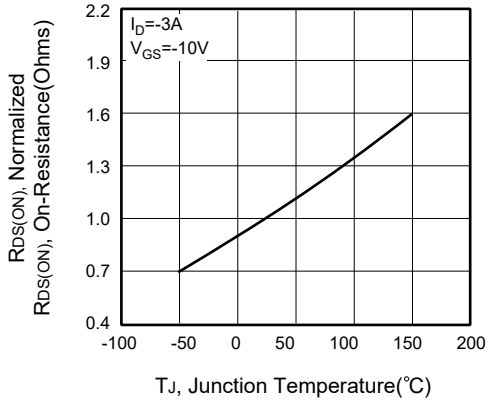


Figure 10. On-Resistance Variation with Temperature

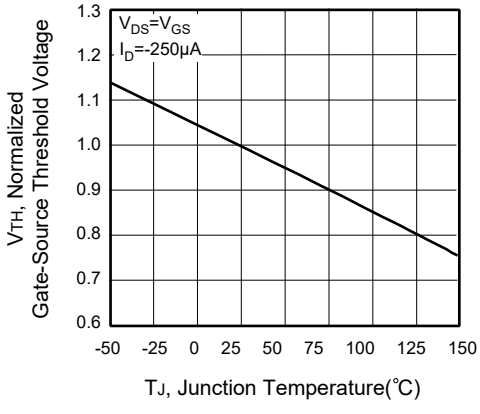


Figure 11. Gate Threshold Variation with Temperature

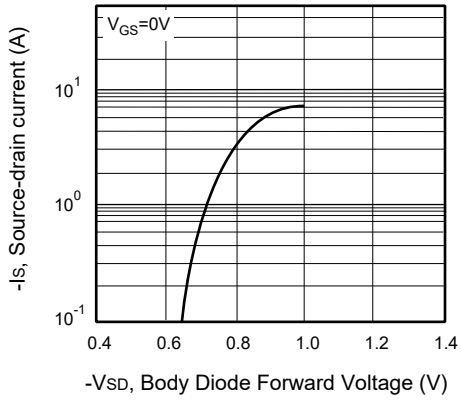


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

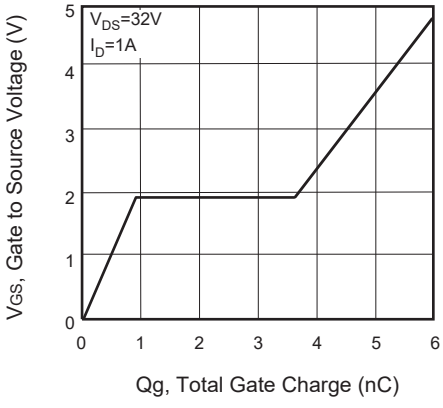


Figure 13. Gate Charge

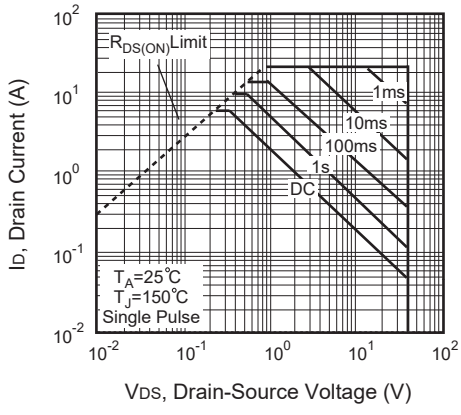


Figure 14. Maximum Safe Operating Area

P-CHANNEL

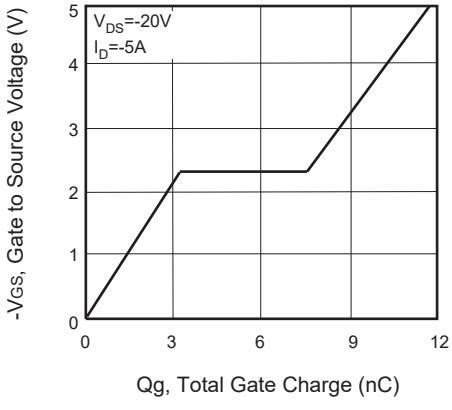


Figure 15. Gate Charge

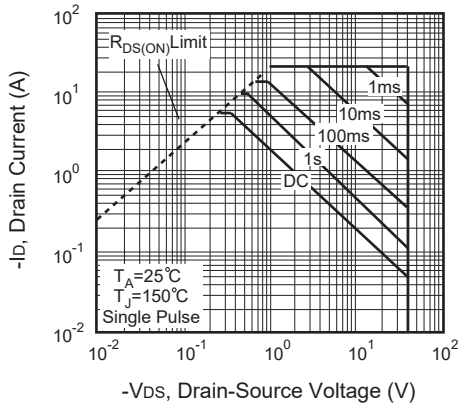


Figure 16. Maximum Safe Operating Area

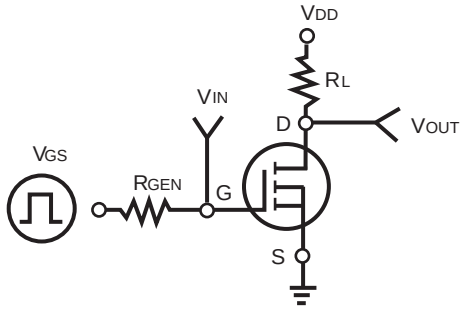


Figure 17. Switching Test Circuit

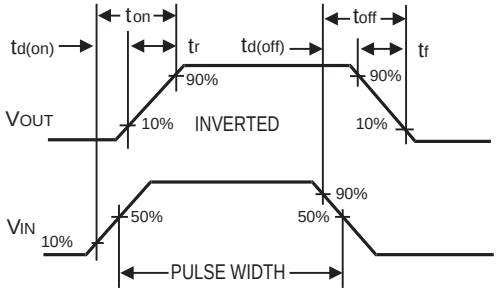


Figure 18. Switching Waveforms

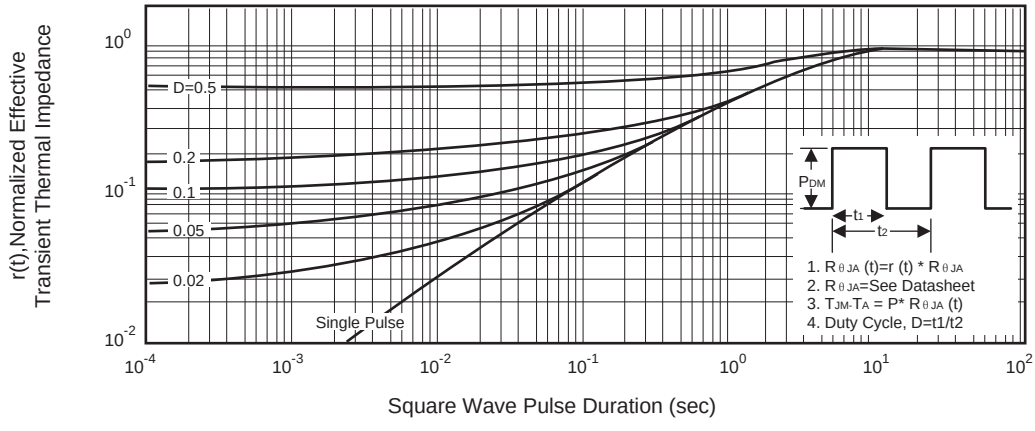
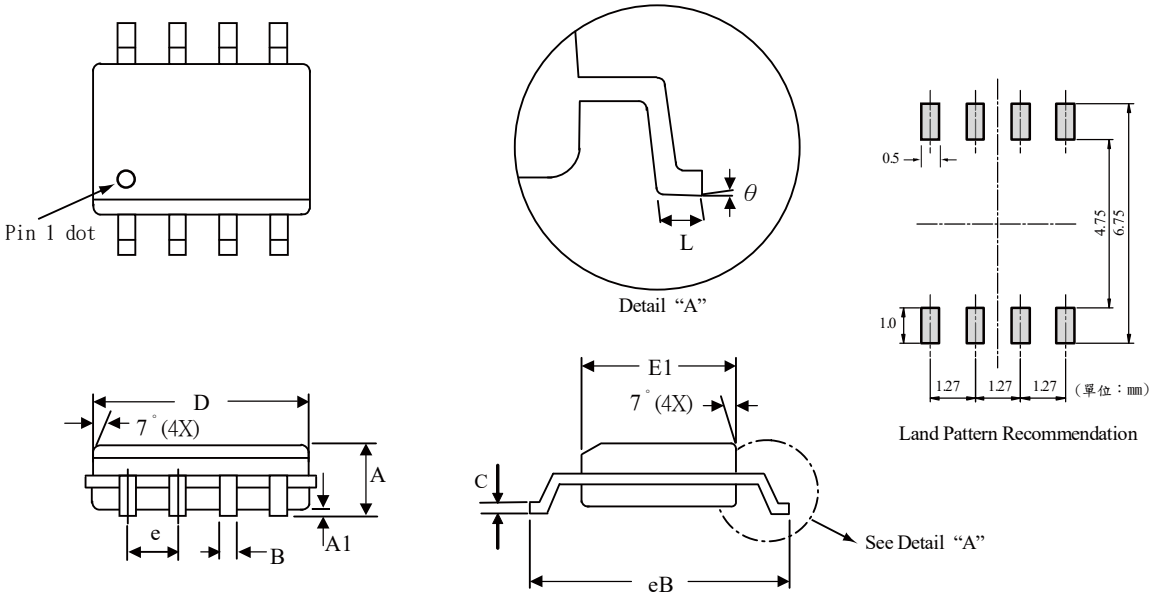


Figure 19. Normalized Thermal Transient Impedance Curve

SO-8 產品外觀尺寸圖 (Product Outline Dimension)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.31	0.51	0.012	0.020
C	0.17	0.25	0.007	0.010
D	4.69	5.00	0.185	0.197
E1	3.70	4.06	0.146	0.160
eB	5.80	6.20	0.228	0.244
e	1.27		0.050	
L	0.40	0.95	0.016	0.037
θ	0°	8°	0°	8°