



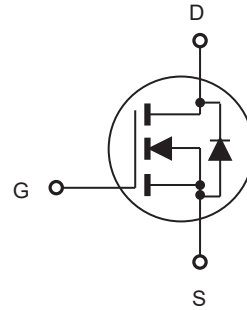
# CEP1188SA/CEB1188SA CEF1188SA

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	$V_{DSS}@T_{Jmax}$	$R_{DS(ON)}$	$I_D$	@ $V_{GS}$
CEP1188SA	900V	0.72 $\Omega$	7.8 A	10V
CEB1188SA	900V	0.72 $\Omega$	7.8 A	10V
CEF1188SA	900V	0.72 $\Omega$	7.8 A <sup>d</sup>	10V

- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	$V_{DS}$	850		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$I_D$	7.8	7.8 <sup>d</sup>	A
		5	5 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}^e$	31.2	31.2 <sup>d</sup>	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	119	39	W
		0.95	0.31	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>g</sup>	$E_{AS}$	172.8		mJ
Single Pulsed Avalanche Current <sup>g</sup>	$I_{AS}$	2.4		A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.05	3.2	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	$^\circ\text{C/W}$



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	850			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 850V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4A$		0.62	0.72	$\Omega$
Gate input resistance	$R_g$	$f=1\text{MHz}, \text{open Drain}$		6.4		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 100V, V_{GS} = 0V, f = 1.0 \text{ MHz}$		685		pF
Output Capacitance	$C_{oss}$			55		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 4A, V_{GS} = 10V, R_{GEN} = 10\Omega$		25		ns
Turn-On Rise Time	$t_r$			9		ns
Turn-Off Delay Time	$t_{d(off)}$			45		ns
Turn-Off Fall Time	$t_f$			10		ns
Total Gate Charge	$Q_g$	$V_{DS} = 640V, I_D = 4A, V_{GS} = 10V$		17		nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			6		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				7.8	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 4A$			1.5	V
Reverse Recovery Time	$T_{rr}$	$I_F = 4A, di/dt = 100A/\mu s$		341.4		ns
Reverse Recovery Charge	$Q_{rr}$			1.89		$\mu C$
Peak Reverse Recovery Current	$I_{rr}$			10.67		A
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 4.5A$ . g.L = 60mH, $I_{AS} = 2.4A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ C$						



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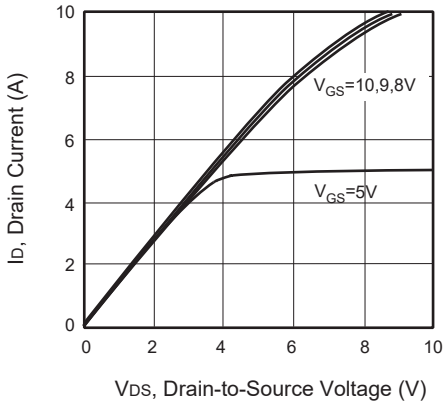


Figure 1. Output Characteristics

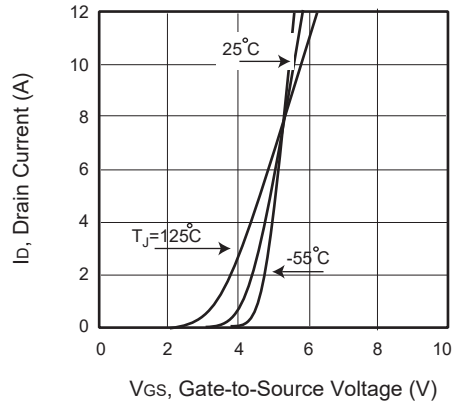


Figure 2. Transfer Characteristics

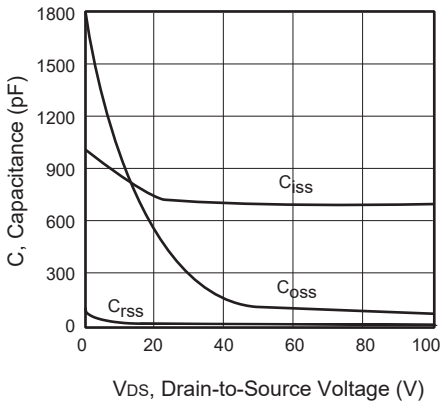


Figure 3. Capacitance

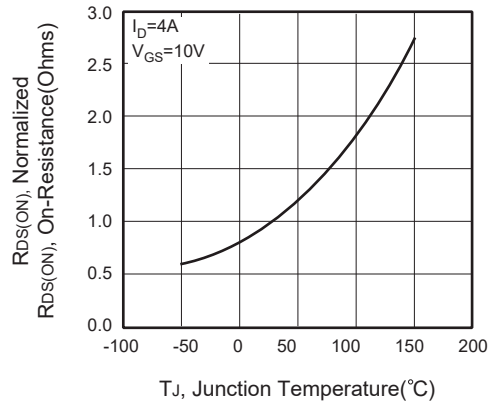


Figure 4. On-Resistance Variation with Temperature

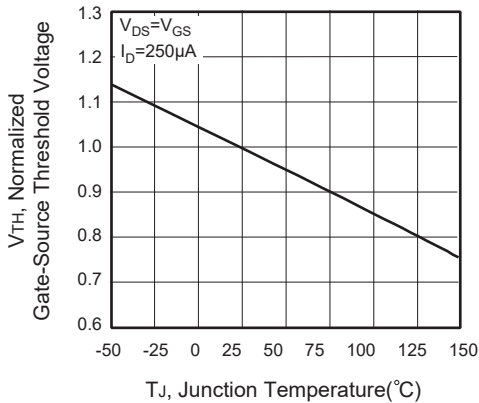


Figure 5. Gate Threshold Variation with Temperature

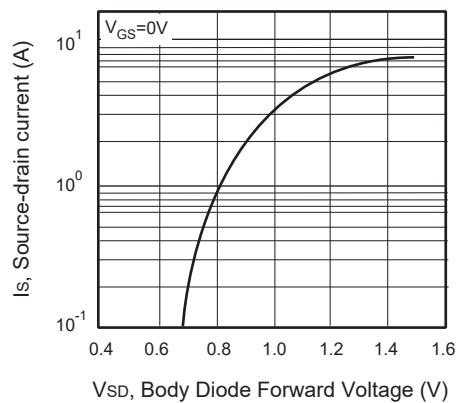
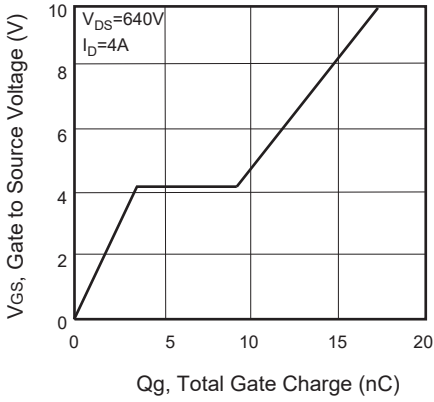
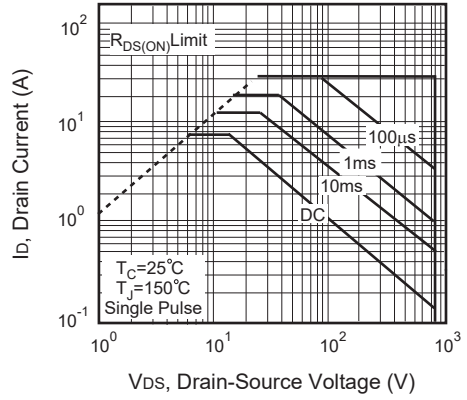


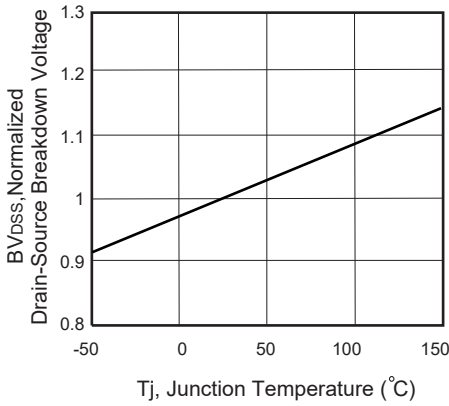
Figure 6. Body Diode Forward Voltage Variation with Source Current



**Figure 7. Gate Charge**



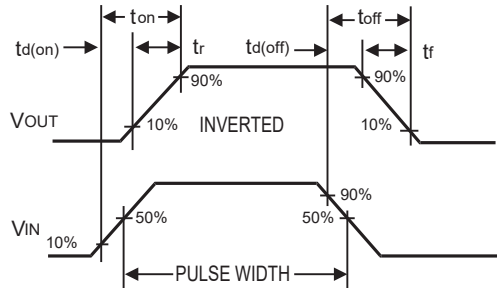
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**



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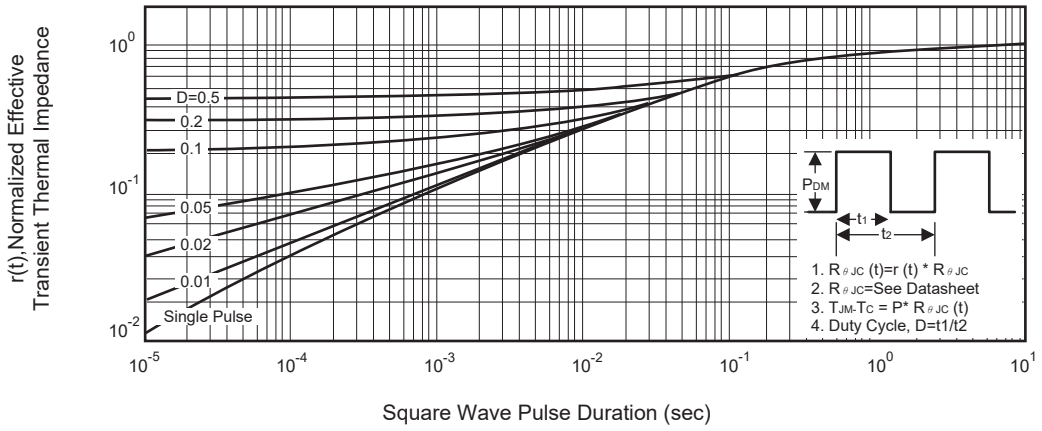


Figure 12. Normalized Thermal Transient Impedance Curve