



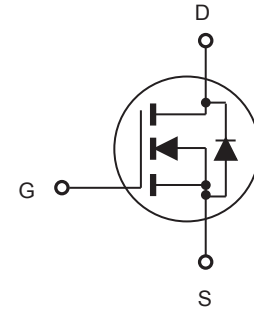
CEP1310SL/CEB1310SL

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- 100V, 88A, $R_{DS(ON)} = 7.5m\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- RoHS compliant.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous @ $T_C = 25^\circ C$	I_D	88	A
Drain Current-Continuous @ $T_C = 100^\circ C$		56	A
Drain Current-Pulsed ^a	I_{DM}	352	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	P_D	104	W
		0.8	W/ $^\circ C$
Single Pulsed Avalanche Energy ^d	E_{AS}	200	mJ
Single Pulsed Avalanche Current ^d	I_{AS}	20	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.2	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

This is preliminary information on a new product in development now
 Details are subject to change without notice .

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<http://www.cet-mos.com>



CEP1310SL/CEB1310SL

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		6.2	7.5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$		8.6	11	$m\Omega$
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1MHz$		1895		pF
Output Capacitance	C_{oss}			405		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 80V, I_D = 20A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		17		ns
Turn-On Rise Time	t_r			9		ns
Turn-Off Delay Time	$t_{d(off)}$			54		ns
Turn-Off Fall Time	t_f			15		ns
Total Gate Charge	Q_g	$V_{DS} = 80V, I_D = 20A,$ $V_{GS} = 4.5V$		22		nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			14		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				86	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 10A$			1.2	V
Notes : a. Repetitive Rating : Pulse width limited by maximum junction temperature. b. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c. Guaranteed by design, not subject to production testing. d. L = 1mH, $I_{AS} = 20A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						

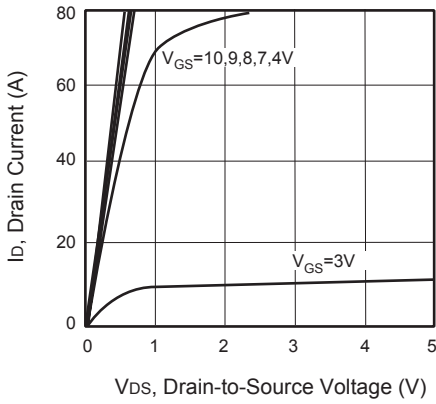


Figure 1. Output Characteristics

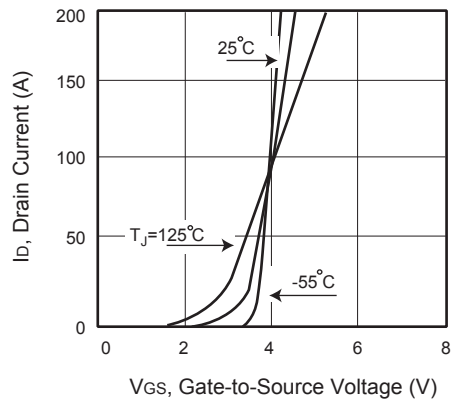


Figure 2. Transfer Characteristics

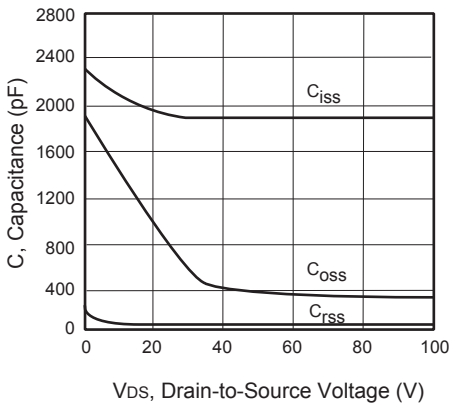


Figure 3. Capacitance

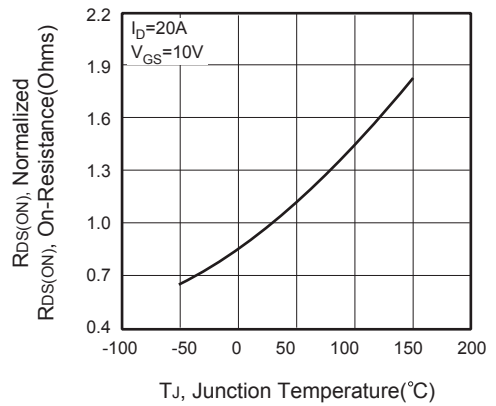


Figure 4. On-Resistance Variation with Temperature

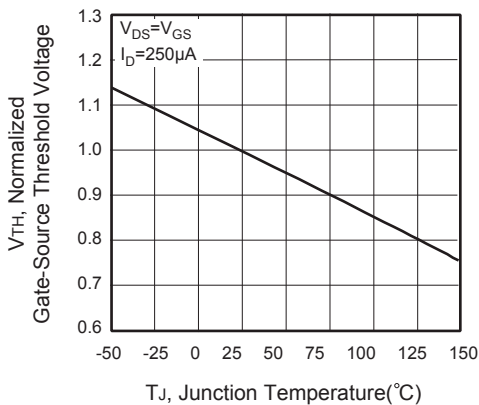


Figure 5. Gate Threshold Variation with Temperature

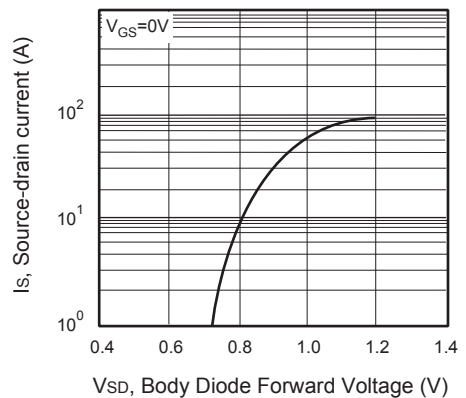


Figure 6. Body Diode Forward Voltage Variation with Source Current

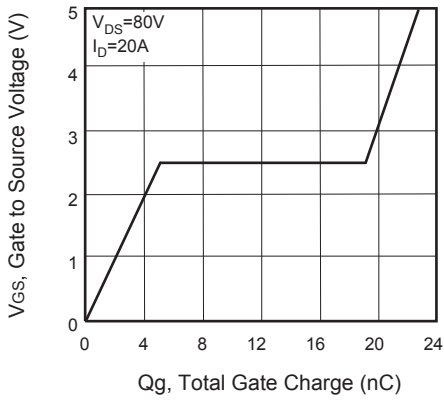


Figure 7. Gate Charge

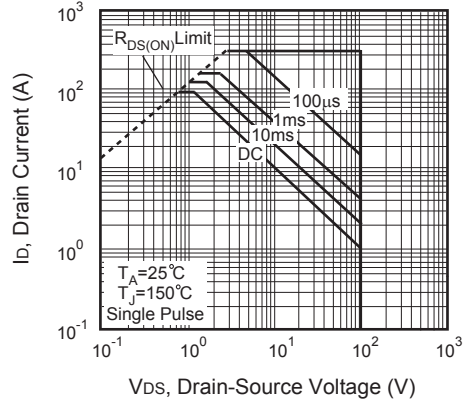


Figure 8. Maximum Safe Operating Area

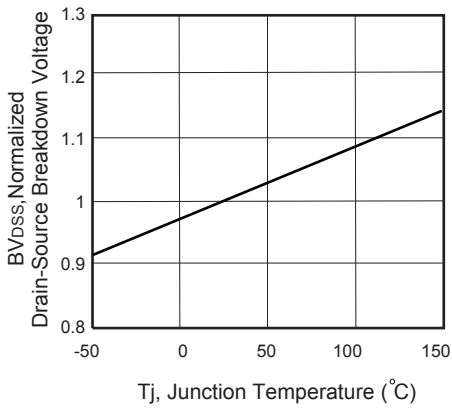


Figure 9. Breakdown Voltage Variation VS Temperature

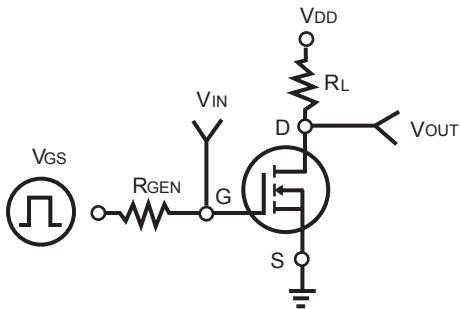


Figure 10. Switching Test Circuit

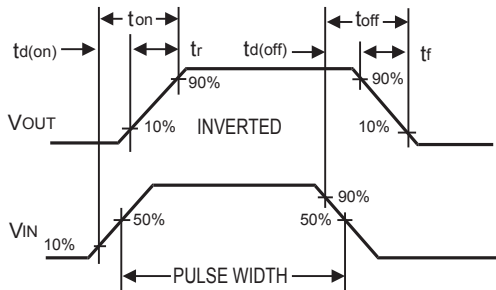


Figure 11. Switching Waveforms

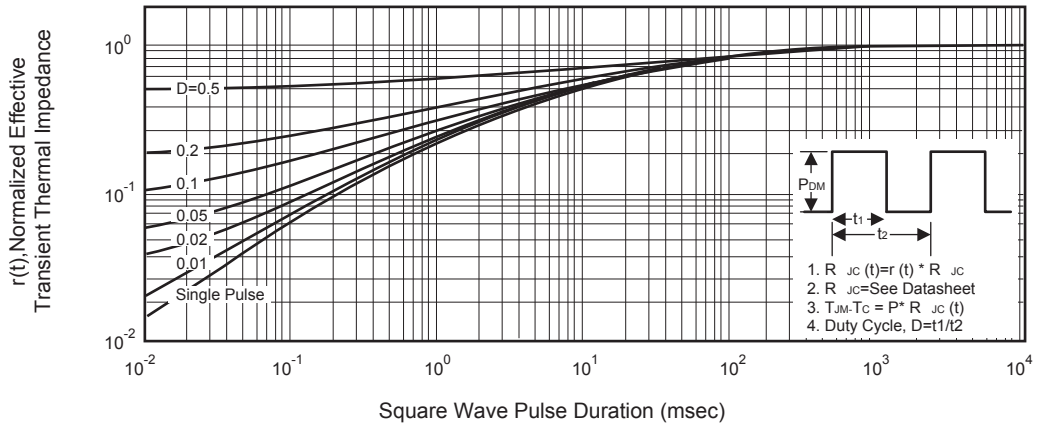


Figure 12. Normalized Thermal Transient Impedance Curve