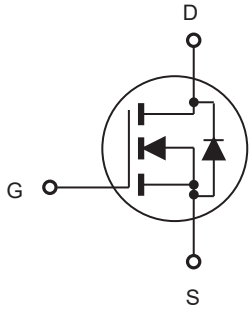
CEP145N10S/CEB145N10S
CEF145N10S

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

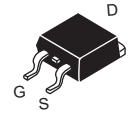
Type	V_{DSS}	$R_{DS(ON)}$	I_D	@V_{GS}
CEP145N10S	100V	4.5mΩ	143A	10V
CEB145N10S	100V	4.5mΩ	143A	10V
CEF145N10S	100V	4.5mΩ	143A [d]	10V



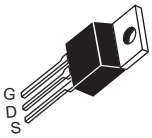
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.

Applications

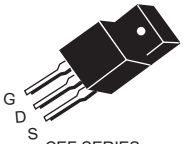
- Synchronous Rectification for SMPS.
- Battery Protection Circuit.



CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F

ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	100		V
Gate-Source Voltage	V_{GS}	± 20		V
Drain Current-Continuous @ T_C = 25℃	I_D	143	143 [d]	A
@ T_C = 100℃		90	90 [d]	A
Drain Current-Pulsed [a]	I_{DM} [e]	572	572 [d]	A
Maximum Power Dissipation @ T_C = 25℃	P_D	166	50	W
- Derate above 25℃		1.32	0.4	W/℃
Single Pulsed Avalanche Energy [g]	E_{AS}	180		mJ
Single Pulsed Avalanche Current [g]	I_{AS}	60		A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		℃

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.75	2.5	℃/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	℃/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A		3.8	4.5	mΩ
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 50V, V_{GS} = 0V, f = 1.0 MHz		2615		pF
Output Capacitance	C_{oss}			750		pF
Reverse Transfer Capacitance	C_{rss}			43		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 80V, I_D = 20A, V_{GS} =10V, R_{GEN} = 6Ω		46		ns
Turn-On Rise Time	t_r			34		ns
Turn-Off Delay Time	$t_{d(off)}$			58		ns
Turn-Off Fall Time	t_f			32		ns
Total Gate Charge	Q_g	V_{DS} = 80V, I_D = 20A, V_{GS} = 10V		71		nC
Gate-Source Charge	Q_{gs}			14		nC
Gate-Drain Charge	Q_{gd}			36		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S [f]				138	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 20A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature .
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2% .
c.Guaranteed by design, not subject to production testing.
d.Limited only by maximum temperature allowed .
e.Pulse width limited by safe operating area .
f.Full package $I_{S(max)}$ = 41A .
g.L = 0.1mH, I_{AS} = 60A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.

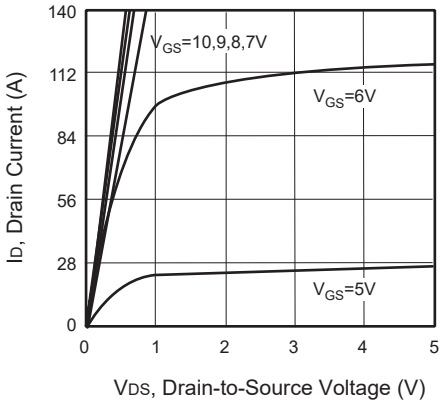


Figure 1. Output Characteristics

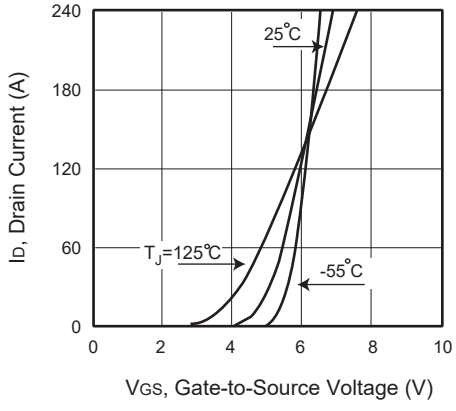


Figure 2. Transfer Characteristics

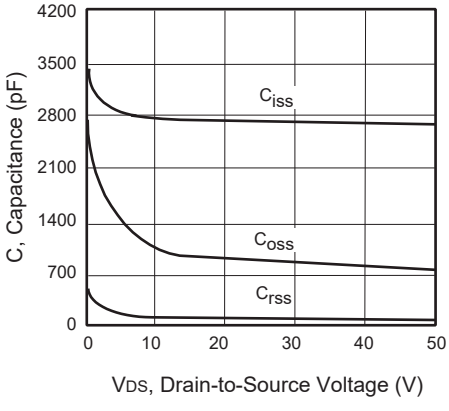


Figure 3. Capacitance

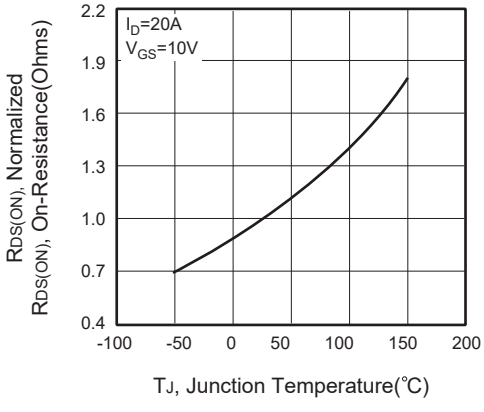


Figure 4. On-Resistance Variation with Temperature

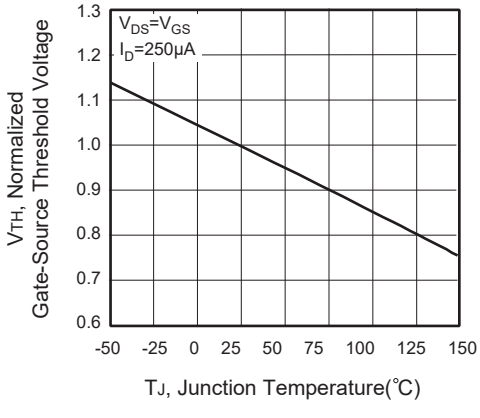


Figure 5. Gate Threshold Variation with Temperature

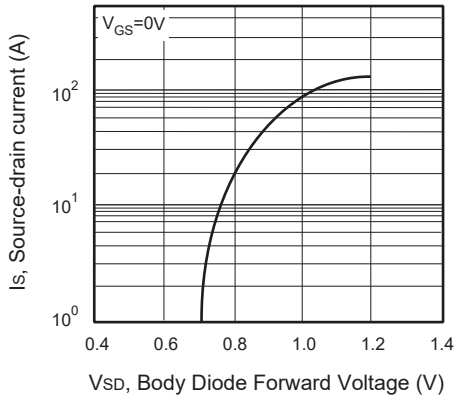


Figure 6. Body Diode Forward Voltage Variation with Source Current

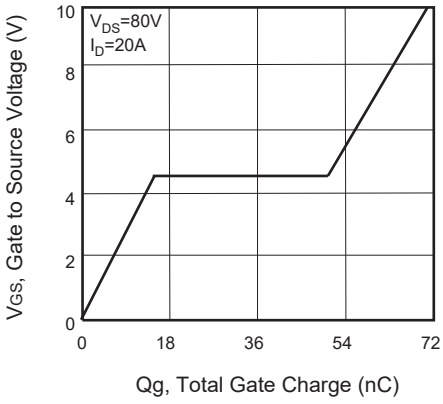


Figure 7. Gate Charge

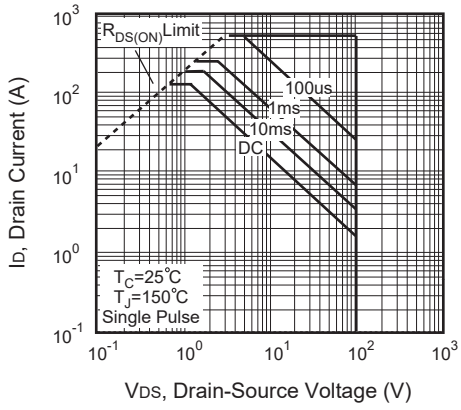


Figure 8. Maximum Safe Operating Area

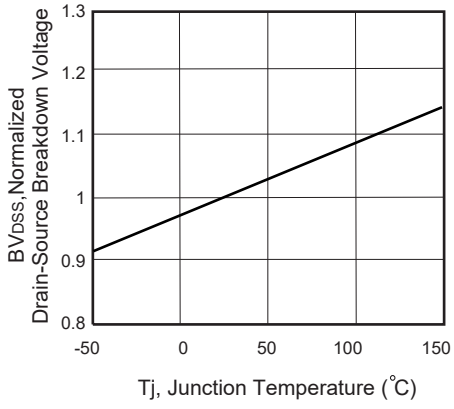


Figure 9. Breakdown Voltage Variation VS Temperature

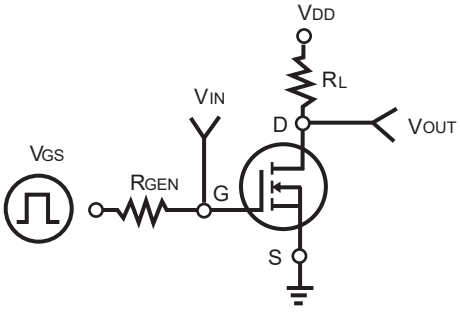


Figure 10. Switching Test Circuit

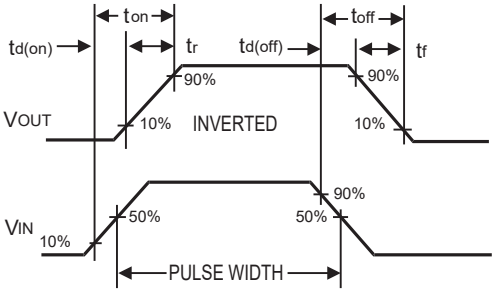


Figure 11. Switching Waveforms

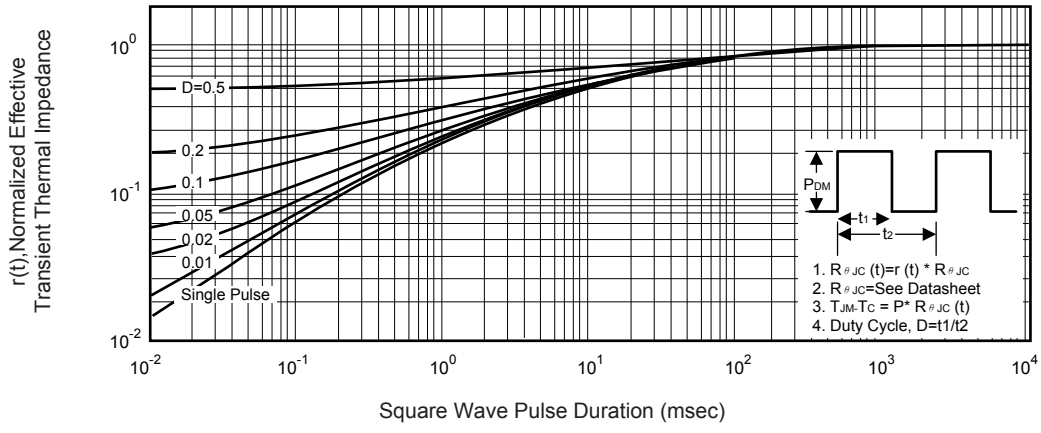


Figure 12. Normalized Thermal Transient Impedance Curve