



CEP16N65/CEB16N65 CEF16N65

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

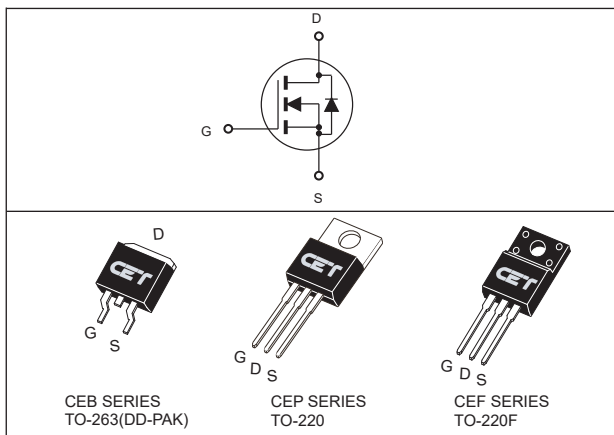
FEATURES

- High power and current handling capability.
- Reliable and rugged.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.

APPLICATIONS

- LED driver.
- Switched mode power supplies.
- Power factor correction.

Type	$V_{DS}@T_{J\max}$	$R_{DS(ON)} \text{ typ } @V_{GS}$	I_D
CEP16N65	650V	$420\text{m}\Omega @V_{GS} = 10\text{V}$	16A
CEB16N65	650V	$420\text{m}\Omega @V_{GS} = 10\text{V}$	16A
CEF16N65	650V	$420\text{m}\Omega @V_{GS} = 10\text{V}$	16A^d



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	16	16^d	A
		10	10^d	A
Drain Current-Pulsed ^a	I_{DM}^e	64	64^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	312	89	W
		2.5	0.7	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^g	E_{AS}	720		mJ
Single Pulsed Avalanche Current ^g	I_{AS}	12		A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.4	1.4	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	$^\circ\text{C}/\text{W}$

This is preliminary information on a new product in development now
Details are subject to change without notice .

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<http://www.cet-mos.com>



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CEF16N65

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 8A$		420	500	m Ω
Gate input resistance	R_g	f=1MHz,open Drain		0.7		Ω
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz		3165		pF
Output Capacitance	C_{oss}			265		pF
Reverse Transfer Capacitance	C_{rss}			10		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325V, I_D = 16A,$ $V_{GS} = 10V, R_{GEN} = 10\Omega$		29		ns
Turn-On Rise Time	t_r			8		ns
Turn-Off Delay Time	$t_{d(off)}$			66		ns
Turn-Off Fall Time	t_f			12		ns
Total Gate Charge	Q_g	$V_{DS} = 520V, I_D = 16A,$ $V_{GS} = 10V$		52		nC
Gate-Source Charge	Q_{gs}			12		nC
Gate-Drain Charge	Q_{gd}			18		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Current-Continuous	I_S ^f				16	A
Drain-Source Diode Current-Pulsed ^b	I_{SM}				64	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 16A$			1.5	V
Reverse Recovery Time	T_{rr}	$I_F = 16A,$ di /dt = 100A/us		465		ns
Reverse Recovery Charge	Q_{rr}			7.5		μC
Notes :						
a.Repetitive Rating : Pulse width limited by maximum junction temperature .						
b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.						
c.Guaranteed by design, not subject to production testing.						
d.Limited only by maximum temperature allowed .						
e.Pulse width limited by safe operating area .						
f.Full package $I_{S(max)} = 8.4A$.						
g.L = 10mH, $I_{AS} = 12A$, $V_{DD} = 60V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						

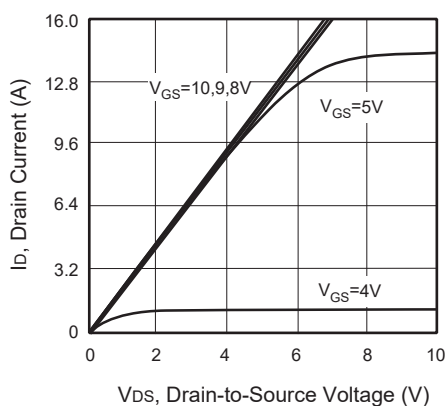


Figure 1. Output Characteristics

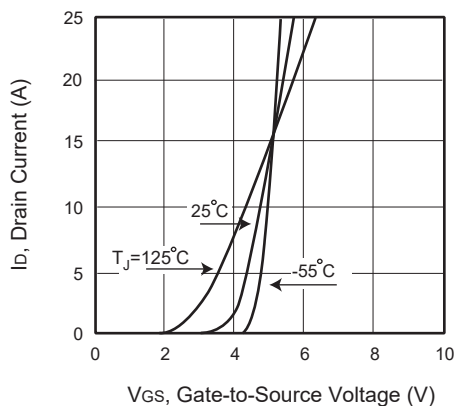


Figure 2. Transfer Characteristics

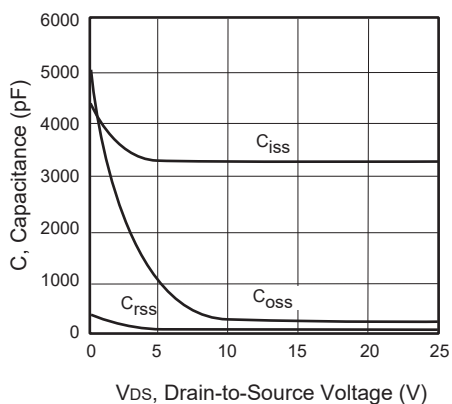


Figure 3. Capacitance

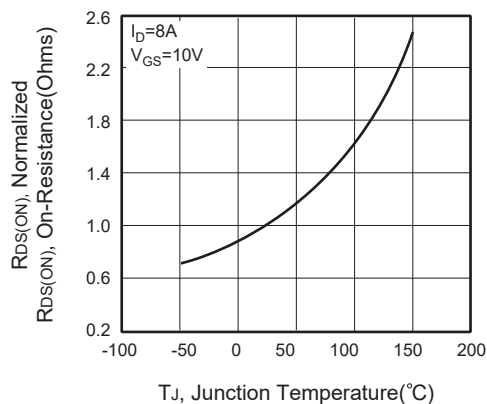


Figure 4. On-Resistance Variation with Temperature

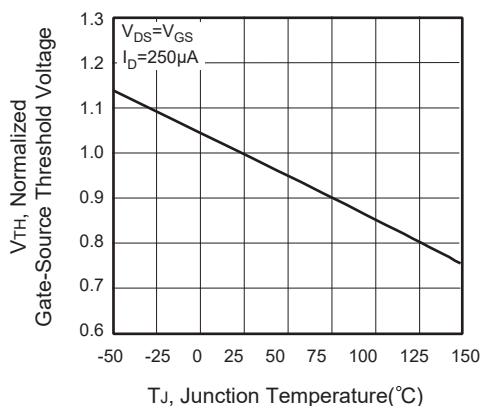


Figure 5. Gate Threshold Variation with Temperature

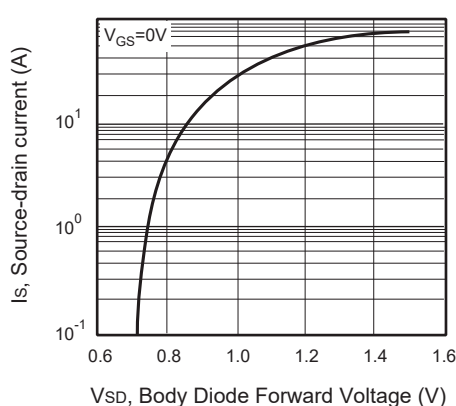


Figure 6. Body Diode Forward Voltage Variation with Source Current

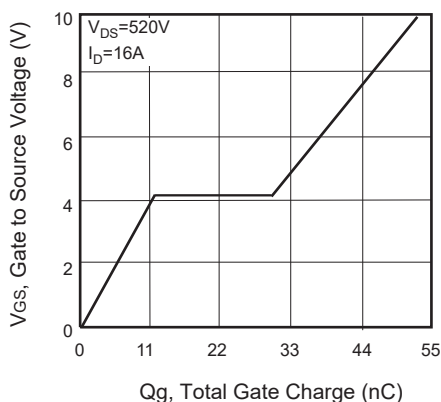


Figure 7. Gate Charge

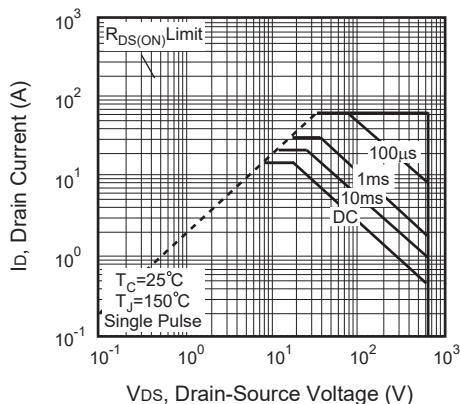


Figure 8. Maximum Safe Operating Area

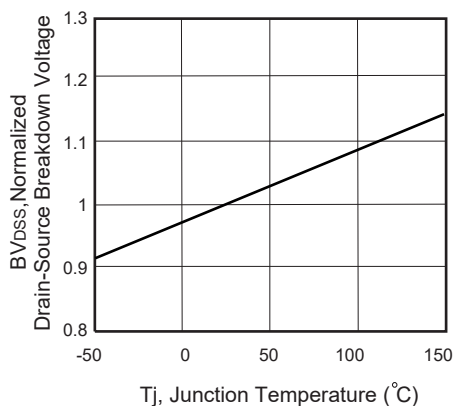


Figure 9. Breakdown Voltage Variation VS Temperature

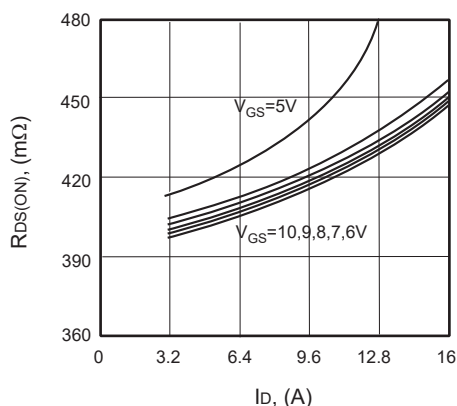


Figure 10. On-Resistance vs. Drain Current

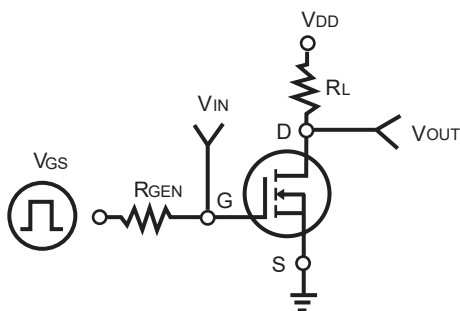


Figure 11. Switching Test Circuit

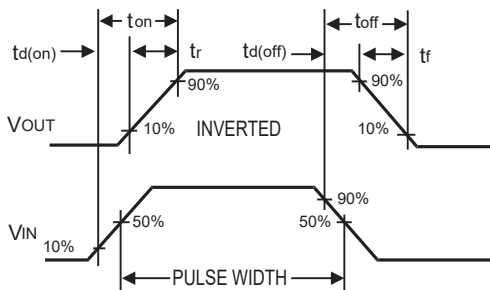


Figure 12. Switching Waveforms

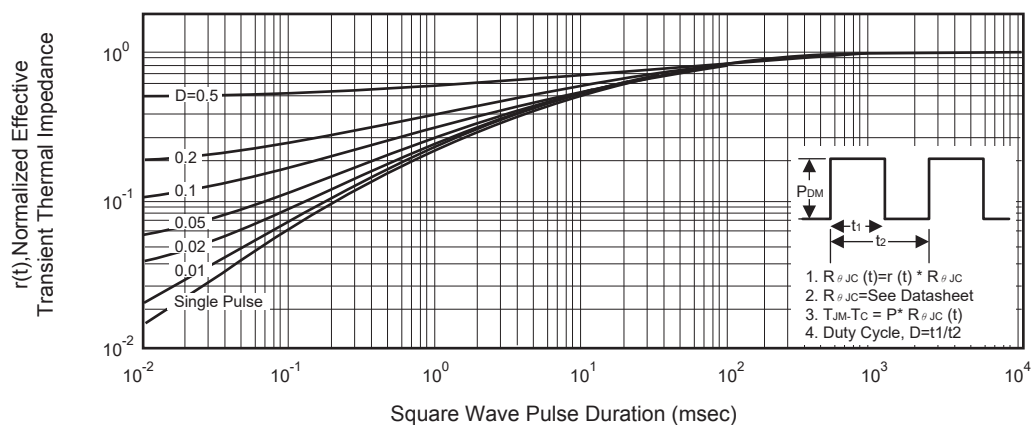


Figure 13. Normalized Thermal Transient Impedance Curve