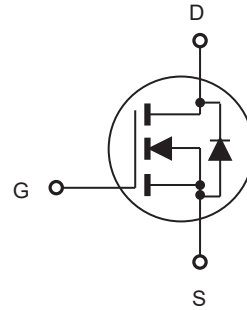
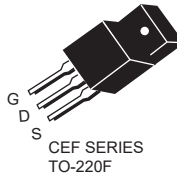


N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP18N5A	500V	0.27Ω	18A	10V
CEB18N5A	500V	0.27Ω	18A	10V
CEF18N5A	500V	0.27Ω	18A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	500		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous @ T _C = 25°C @ T _C = 100°C	I _D	18	18 ^d	A
		11	11 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	72	72 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	208	66	W
		1.6	0.5	W/°C
Single Pulsed Avalanche Energy ^e	E _{AS}	859		mJ
Single Pulsed Avalanche Current ^e	I _{AS}	18		A
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θC}	0.6	1.9	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W



CEP18N5A/CEB18N5A CEF18N5A

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 9A$		0.24	0.27	Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		2465		pF
Output Capacitance	C_{oss}			300		pF
Reverse Transfer Capacitance	C_{rss}			10		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 18A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		36		ns
Turn-On Rise Time	t_r			28		ns
Turn-Off Delay Time	$t_{d(off)}$			78		ns
Turn-Off Fall Time	t_f			11		ns
Total Gate Charge	Q_g	$V_{DS} = 400V, I_D = 18A,$ $V_{GS} = 10V$		58		nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			23		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				18	A
Drain-Source Diode Forward Voltage ^b	V_{SD}^g	$V_{GS} = 0V, I_S = 18A$			1.4	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 10A$. g.Full package V_{SD} test condition $I_S = 10A$. e.L = 5.3mH, $I_{AS} = 18A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25 \text{ C}$						



CEP18N5A/CEB18N5A CEF18N5A

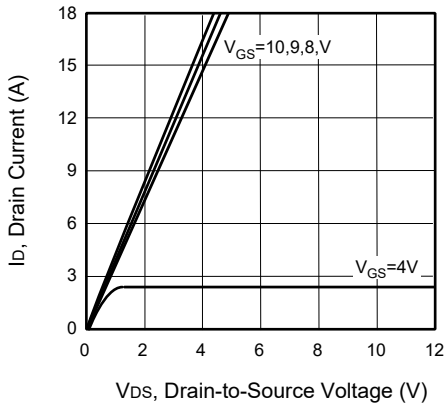


Figure 1. Output Characteristics

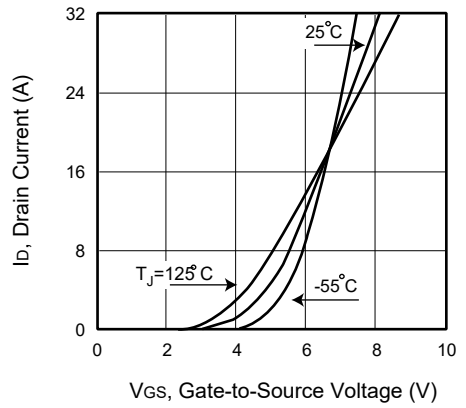


Figure 2. Transfer Characteristics

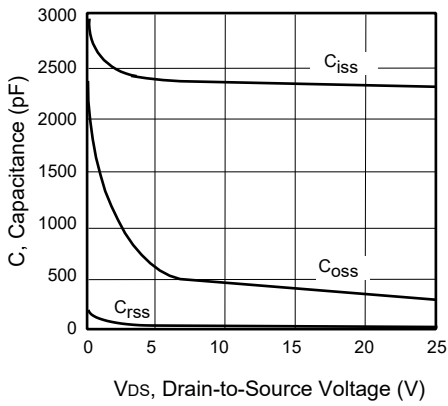


Figure 3. Capacitance

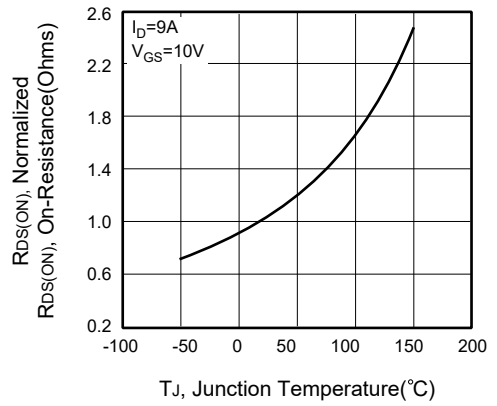


Figure 4. On-Resistance Variation with Temperature

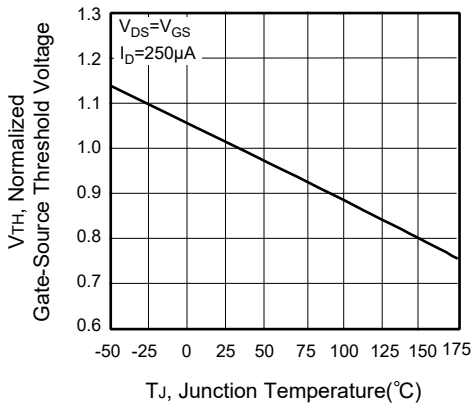


Figure 5. Gate Threshold Variation with Temperature

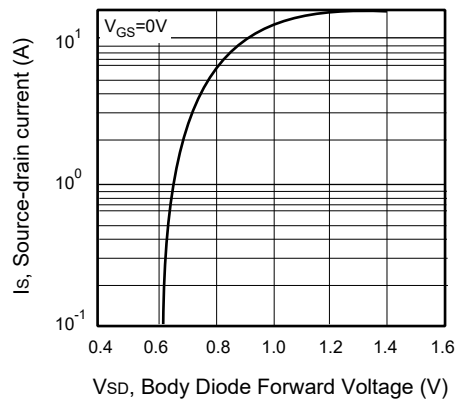


Figure 6. Body Diode Forward Voltage Variation with Source Current

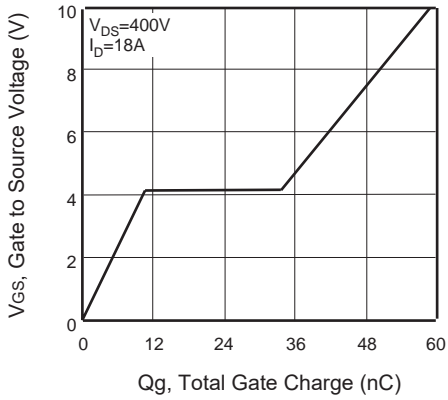


Figure 7. Gate Charge

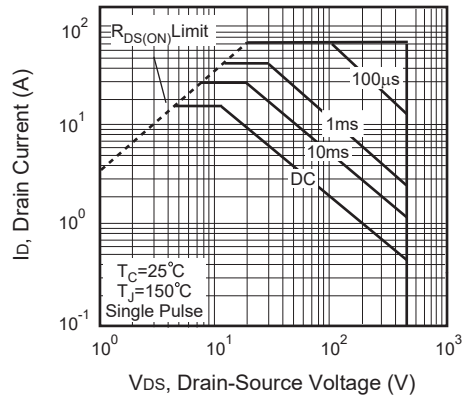


Figure 8. Maximum Safe Operating Area

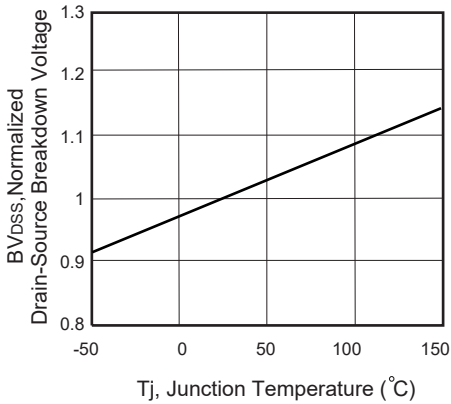


Figure 9. Breakdown Voltage Variation VS Temperature

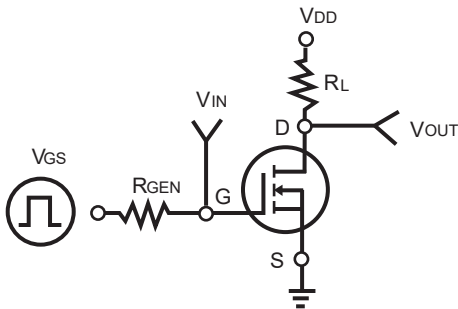


Figure 10. Switching Test Circuit

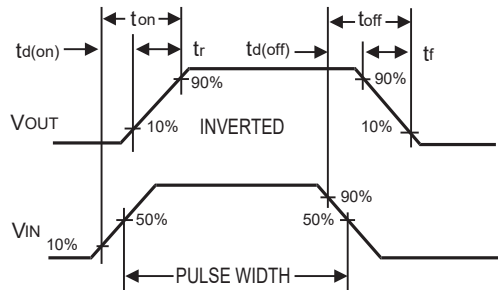


Figure 11. Switching Waveforms



CEP18N5A/CEB18N5A CEF18N5A

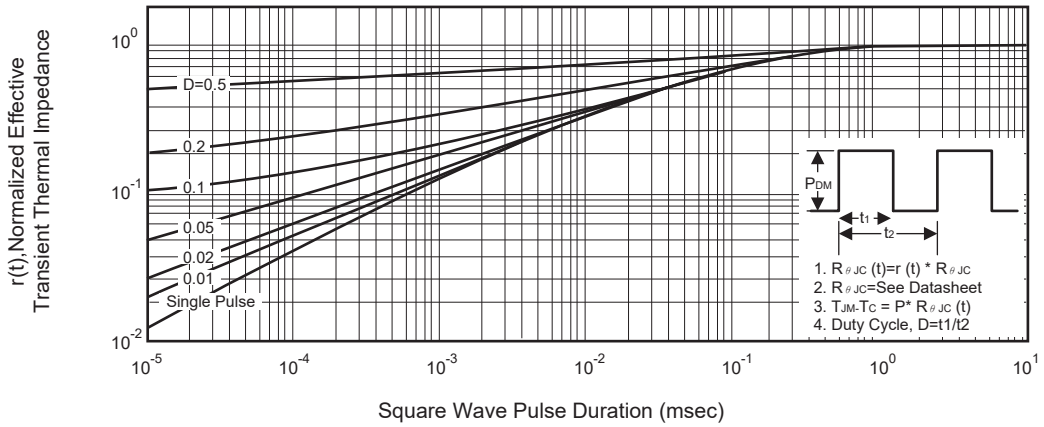


Figure 12. Normalized Thermal Transient Impedance Curve