

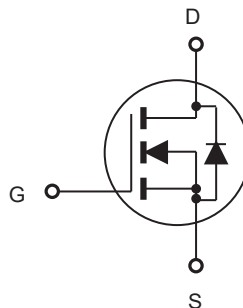
N-Channel Enhancement Mode Field Effect Transistor With Fast Body Diode

PRELIMINARY

FEATURES

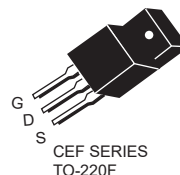
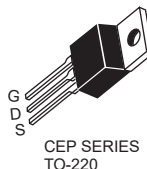
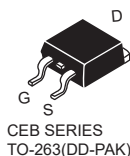
Type	$V_{DSS}@T_{Jmax}$	$R_{DS(ON)}$	I_D	@ V_{GS}
CEP1988SF	900V	160m Ω	26A	10V
CEB1988SF	900V	160m Ω	26A	10V
CEF1988SF	900V	160m Ω	26A ^d	10V

- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Fast reverse recovery time.



APPLICATIONS

- Adapter.
- EV Charging.
- SMPS.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	850		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	26	26 ^d	A
		16	16 ^d	A
Drain Current-Pulsed ^a	I_{DM}^e	104	104 ^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	278	83	W
		2.22	0.66	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^g	E_{AS}	843		mJ
Single Pulsed Avalanche Current ^g	I_{AS}	7.5		A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.45	1.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	$^\circ\text{C}/\text{W}$



CEP1988SF/CEB1988SF CEF1988SF

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	850			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 850V, V_{GS} = 0V$			5	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	3	4	5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10A$		137	160	m Ω
Gate Input Resistance	R_g	f=1MHz, open Drain		3.6		Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		3455		pF
Output Capacitance	C_{oss}			100		pF
Reverse Transfer Capacitance	C_{rss}			5		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 2A,$ $V_{GS} = 10V, R_{GEN} = 4.7\Omega$		43		ns
Turn-On Rise Time	t_r			7		ns
Turn-Off Delay Time	$t_{d(off)}$			130		ns
Turn-Off Fall Time	t_f			48		ns
Total Gate Charge	Q_g		$V_{DS} = 640V, I_D = 7A,$ $V_{GS} = 10V$		70	
Gate-Source Charge	Q_{gs}			16		nC
Gate-Drain Charge	Q_{gd}			29		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				26	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 10A$			1.2	V
Reverse Recovery Time	T_{rr}	$I_F = 10A, di/dt = 100A/\mu s$		176		ns
Reverse Recovery Charge	Q_{rr}			0.94		μC
Peak Reverse Recovery Current	I_{rr}			10.5		A
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 14A$. g.L = 30mH, $I_{AS} = 7.5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						

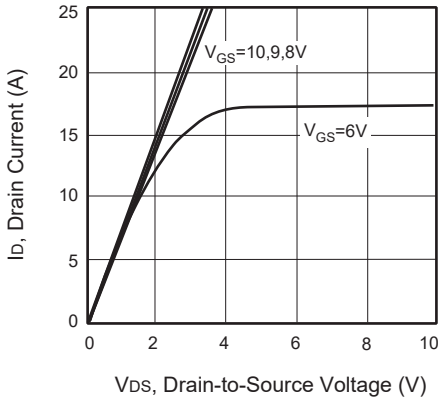


Figure 1. Output Characteristics

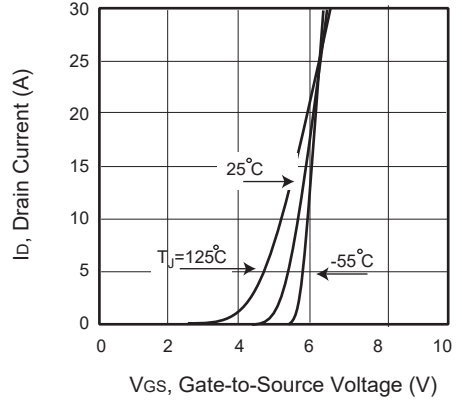


Figure 2. Transfer Characteristics

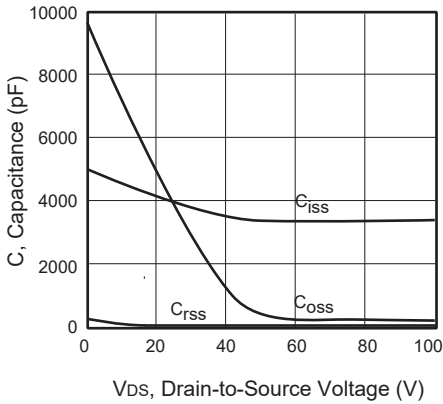


Figure 3. Capacitance

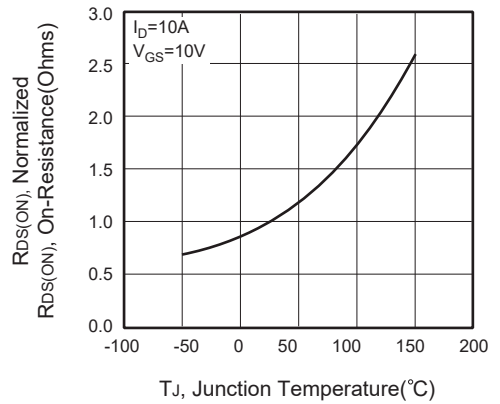


Figure 4. On-Resistance Variation with Temperature

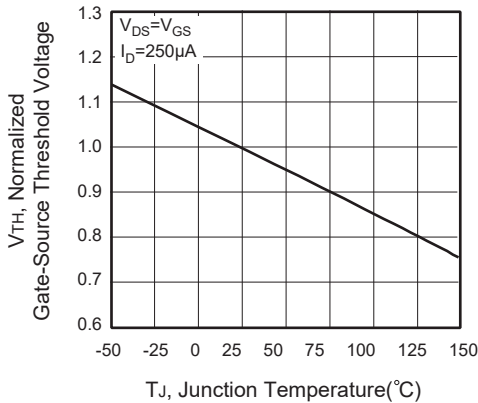


Figure 5. Gate Threshold Variation with Temperature

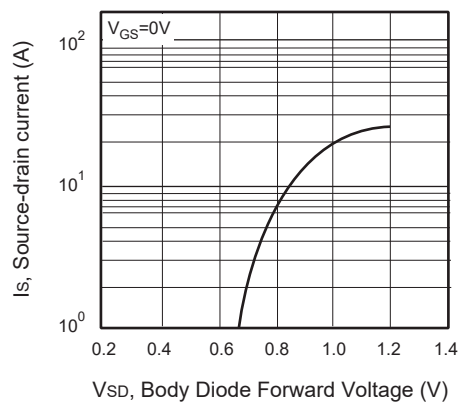


Figure 6. Body Diode Forward Voltage Variation with Source Current

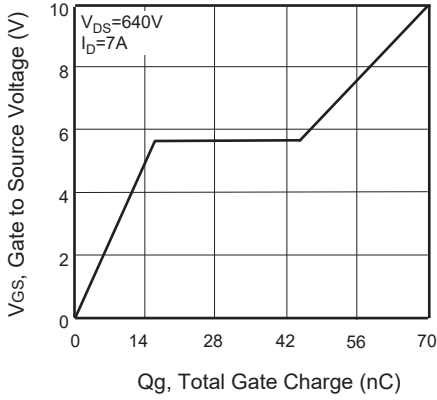


Figure 7. Gate Charge

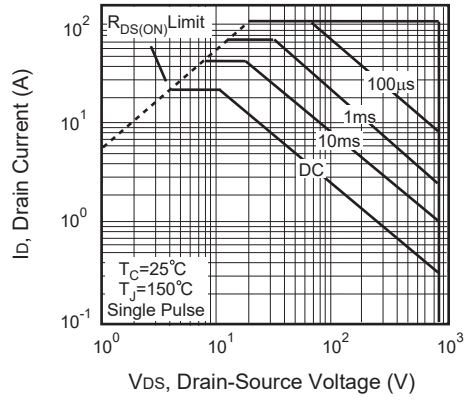


Figure 8. Maximum Safe Operating Area



Figure 9. Breakdown Voltage Variation VS Temperature



Figure 10. Switching Test Circuit

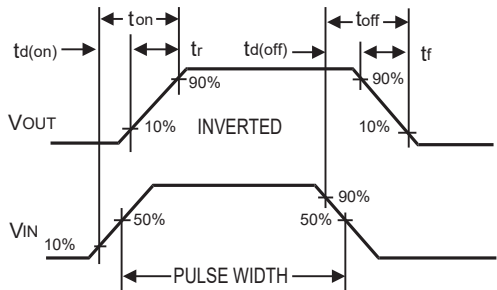


Figure 11. Switching Waveforms

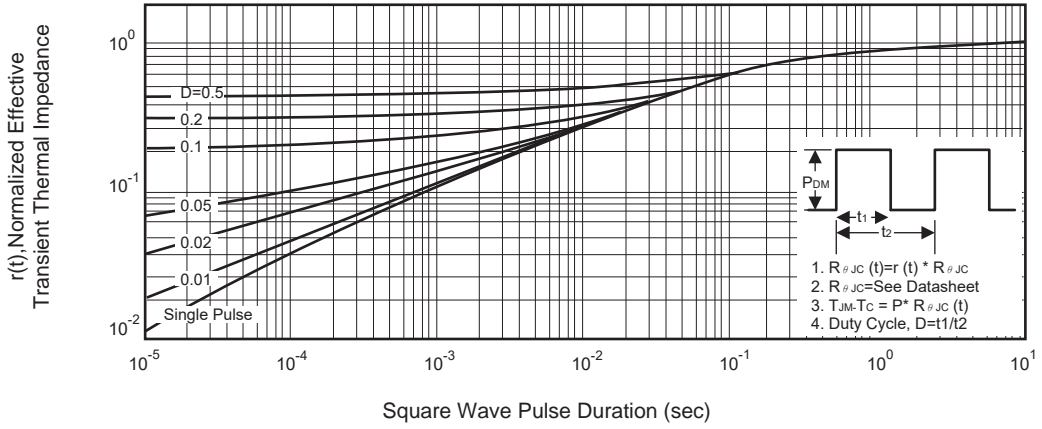


Figure 12. Normalized Thermal Transient Impedance Curve