

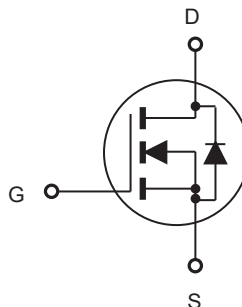


CEP19N65SF/CEB19N65SF CEF19N65SF

N-Channel Enhancement Mode Field Effect Transistor With Fast Body Diode

FEATURES

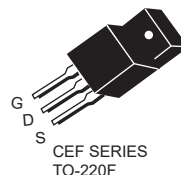
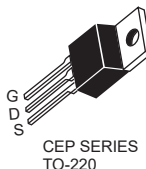
Type	$V_{DSS}@T_{Jmax}$	$R_{DS(ON)}$	I_D	@ V_{GS}
CEP19N65SF	700V	160m Ω	19.3A	10V
CEB19N65SF	700V	160m Ω	19.3A	10V
CEF19N65SF	700V	160m Ω	19.3A ^d	10V



- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Fast reverse recovery time.

APPLICATIONS

- Switch Mode Power Supply (SMPS).
- PWM Motor Controls.
- LED Lighting.
- Adapter.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	19.3	19.3 ^d	A
		12.2	12.2 ^d	A
Drain Current-Pulsed ^a	I_{DM}^e	77.2	77.2 ^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	125	40	W
		1	0.32	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^g	E_{AS}	405		mJ
Single Pulsed Avalanche Current ^g	I_{AS}	9		A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1	3.1	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	$^\circ\text{C}/\text{W}$



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			10	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.5		4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 9.5A$		131	160	m Ω
Gate input resistance	R_g	f=1MHz, open Drain		4.8		Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 200V, V_{GS} = 0V,$ $f = 1MHz$		1555		pF
Output Capacitance	C_{oss}			70		pF
Reverse Transfer Capacitance	C_{rss}			15		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325V, I_D = 19A,$ $V_{GS} = 10V, R_{GEN} = 10\Omega$		33		ns
Turn-On Rise Time	t_r			9		ns
Turn-Off Delay Time	$t_{d(off)}$			61		ns
Turn-Off Fall Time	t_f			7		ns
Total Gate Charge	Q_g	$V_{DS} = 520V, I_D = 19A,$ $V_{GS} = 10V$		29		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			12		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				19.3	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 19A$			1.4	V
Reverse Recovery Time	T_{rr}	$I_F = 19A, di/dt = 100A/us$		165		ns
Reverse Recovery Charge	Q_{rr}			976		nC
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 10.9A$. g.L = 10mH, $I_{AS} = 9A, V_{DD} = 100V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$.						



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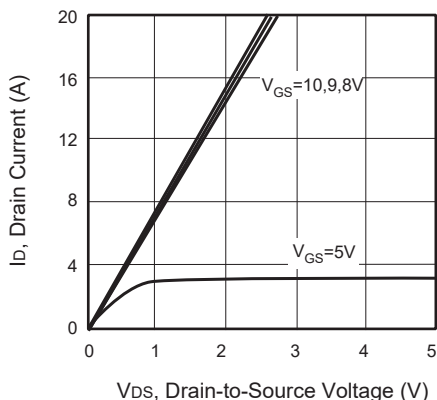


Figure 1. Output Characteristics

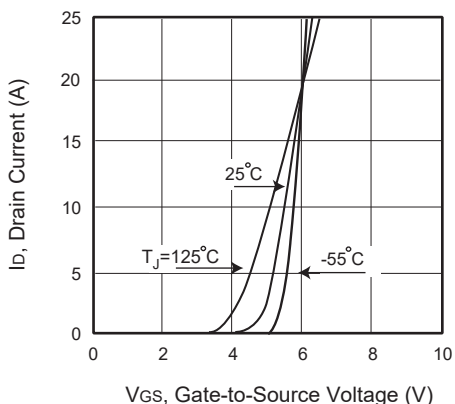


Figure 2. Transfer Characteristics

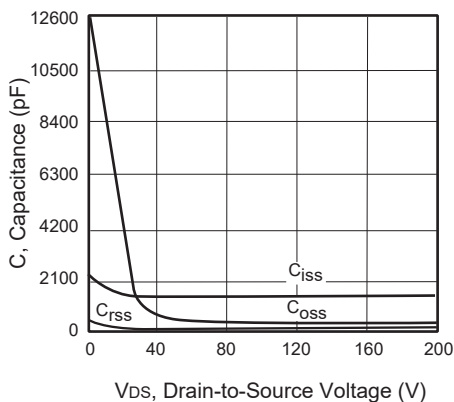


Figure 3. Capacitance

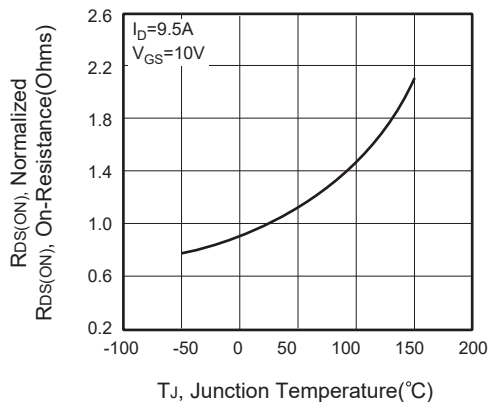


Figure 4. On-Resistance Variation with Temperature

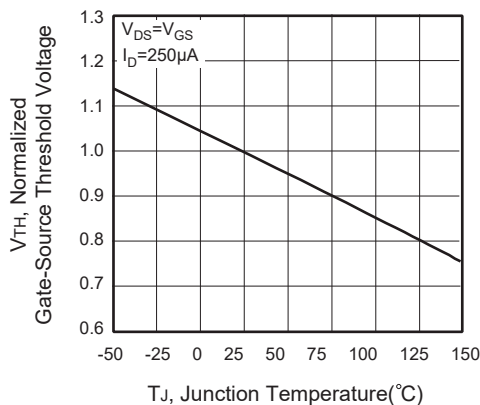


Figure 5. Gate Threshold Variation with Temperature

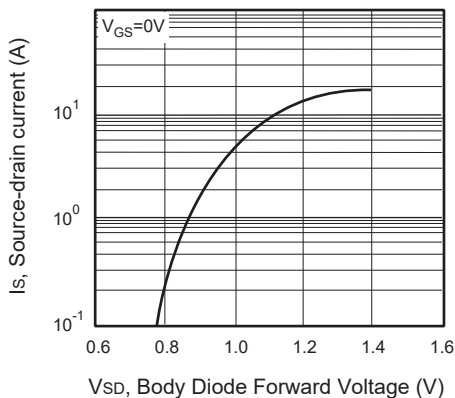


Figure 6. Body Diode Forward Voltage Variation with Source Current

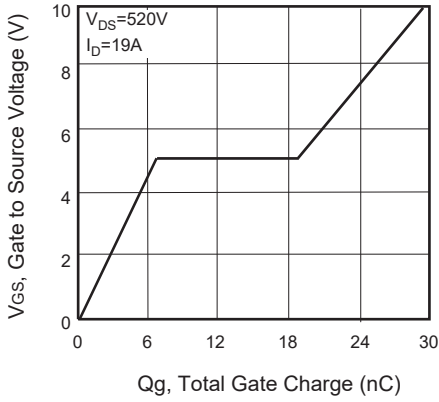


Figure 7. Gate Charge

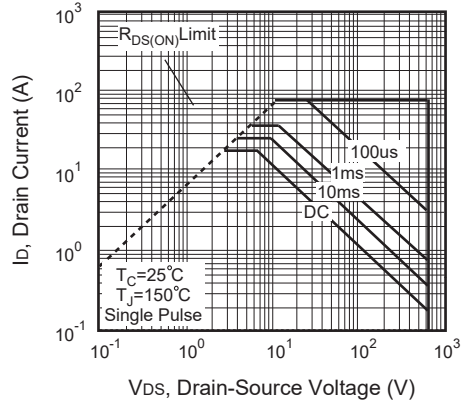


Figure 8. Maximum Safe Operating Area

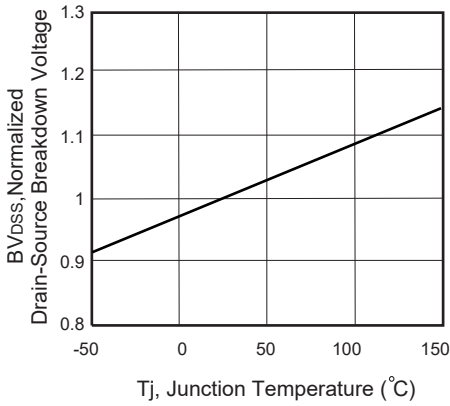


Figure 9. Breakdown Voltage Variation VS Temperature



Figure 10. Switching Test Circuit

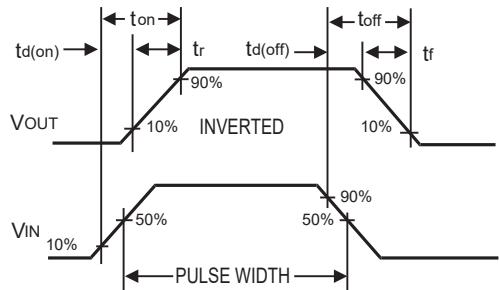


Figure 11. Switching Waveforms



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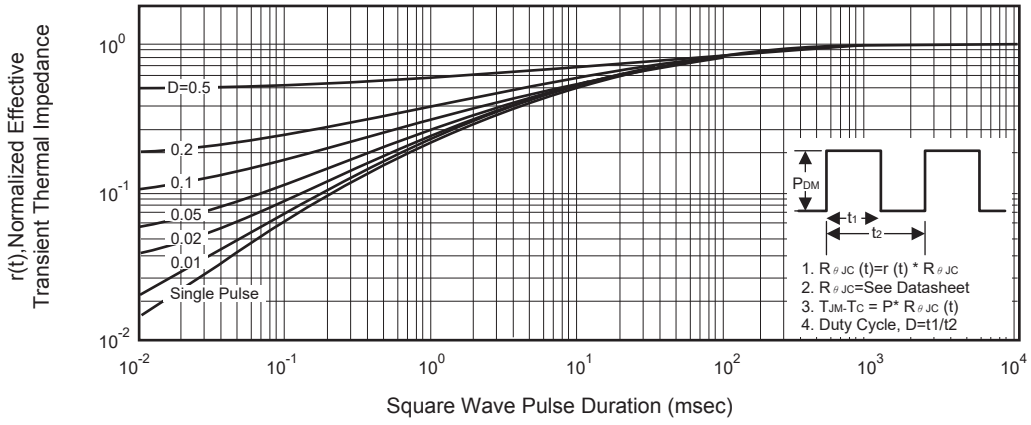


Figure 12. Normalized Thermal Transient Impedance Curve