CEP20N65SA/CEB20N65SA
CEF20N65SA

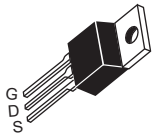
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

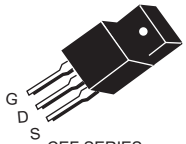
Type	V_{DSS}@$T_{J\ max}$	$R_{DS(ON)}$	I_D	@V_{GS}
CEP20N65SA	700V	0.18Ω	20A	10V
CEB20N65SA	700V	0.18Ω	20A	10V
CEF20N65SA	700V	0.18Ω	20A [d]	10V

- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.

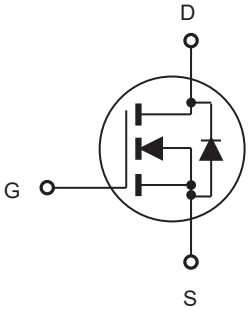
CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current-Continuous @ T_C = 25°C	I_D	20	20 [d]	A
@ T_C = 100°C		13	13 [d]	A
Drain Current-Pulsed [a]	I_{DM} [e]	80	80 [d]	A
Maximum Power Dissipation @ T_C = 25°C	P_D	205	35	W
- Derate above 25°C		1.64	0.28	W/°C
Single Pulsed Avalanche Energy [h]	E_{AS}	607.5		mJ
Single Pulsed Avalanche Current [h]	I_{AS}	4.5		A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.61	3.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 30V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -30V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A		0.15	0.18	Ω
Gate input resistance	R_g	f=1MHz,open Drain		4.7		Ω
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 150V, V_{GS}=0V, f = 1.0 MHz		1570		pF
Output Capacitance	C_{oss}			95		pF
Reverse Transfer Capacitance	C_{rss}			15		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 520V, I_D = 10A, V_{GS} = 10V, R_{GEN} = 6Ω		29		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off Delay Time	$t_{d(off)}$			76		ns
Turn-Off Fall Time	t_f			8		ns
Total Gate Charge	Q_g	V_{DS} = 520V, I_D = 10A, V_{GS} = 10V		42		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			15		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S [f]				20	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 20A[g]			1.5	V
Reverse Recovery Time	T_{rr}	I_D = 20A, di/dt =100A/us		257		ns
Reverse Recovery Charge	Q_{rr}			3.04		μC
Peak Reverse Recovery Current	I_{rr}			22		A
Maximum diode commutation speed	di_F/dt	V_{DS} = 0...400V, I_{SD}< = 20A $T_{j=}$ 25°C			1100	A/μs
Reverse diode dv/dt ruggedness, V_{DS} = 0...480V , I_{SD} < I_D	dv/dt	I_{DR} = 10A, V_{GS} = 0V, V_{DD} = 400V			50	V/ns
MOSFET dv/dt ruggedness, V_{DS} = 0...480V					160	V/ns

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature .
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2% .
c.Guaranteed by design, not subject to production testing.
d.Limited only by maximum temperature allowed .
e.Pulse width limited by safe operating area .
f.Full package $I_{S(max)}$ = 8A .
g.Full package V_{SD} test condition I_S = 8A .
h.L = 60mH, I_{AS} =4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25 C.

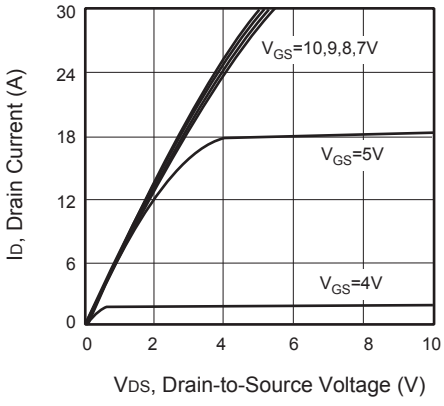


Figure 1. Output Characteristics

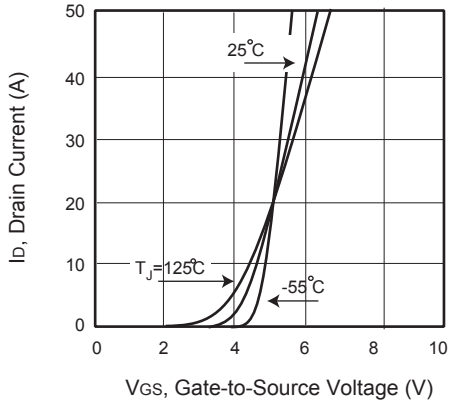


Figure 2. Transfer Characteristics

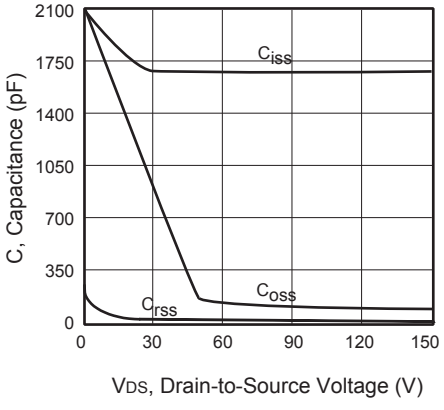


Figure 3. Capacitance

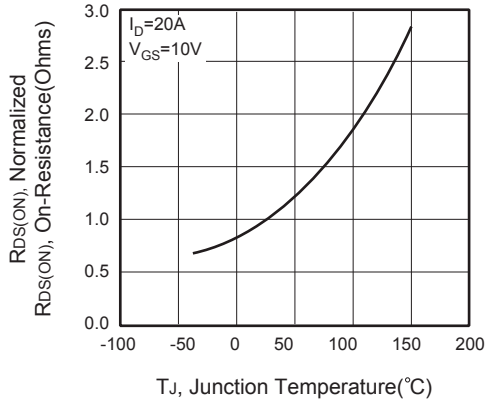


Figure 4. On-Resistance Variation with Temperature

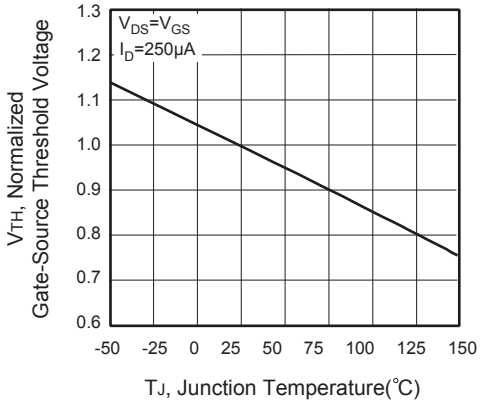


Figure 5. Gate Threshold Variation with Temperature

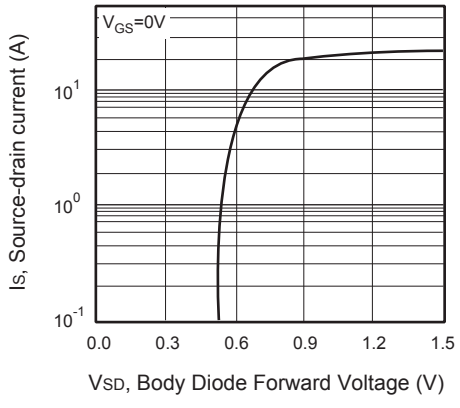


Figure 6. Body Diode Forward Voltage Variation with Source Current

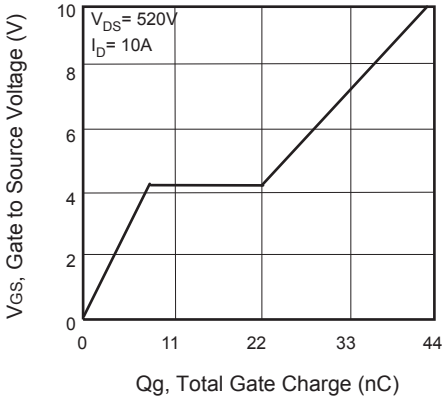


Figure 7. Gate Charge

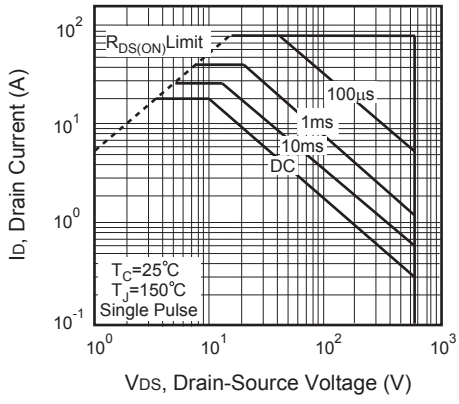


Figure 8. Maximum Safe Operating Area

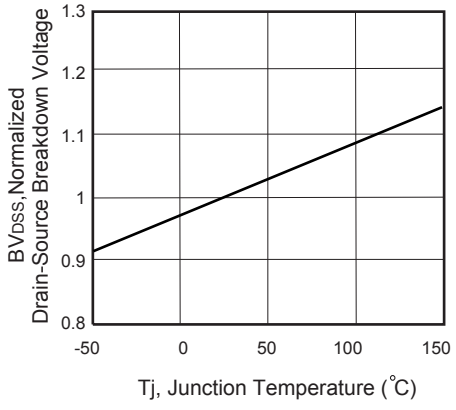


Figure 9. Breakdown Voltage Variation VS Temperature

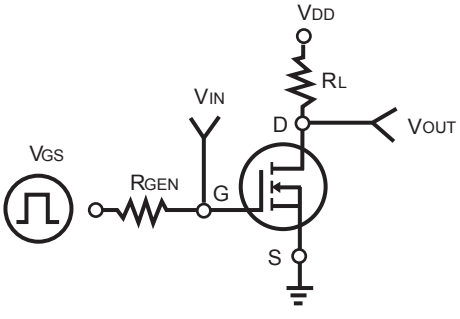


Figure 10. Switching Test Circuit

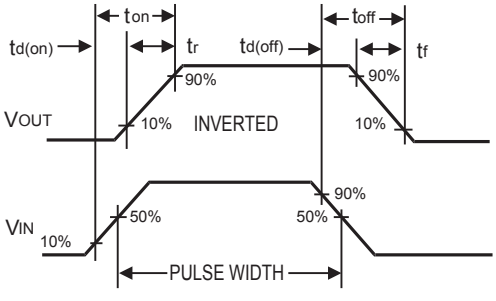


Figure 11. Switching Waveforms

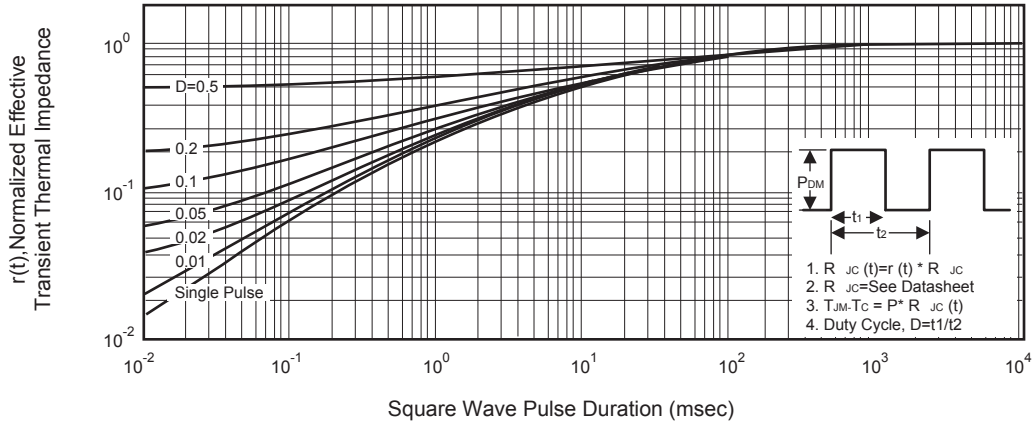


Figure 12. Normalized Thermal Transient Impedance Curve