



CEP38N65SF/CEB38N65SF CEF38N65SF

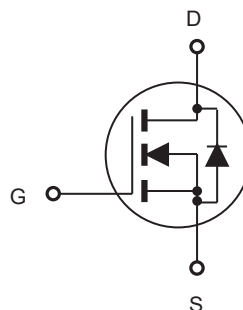
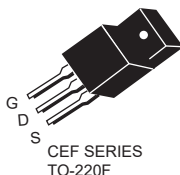
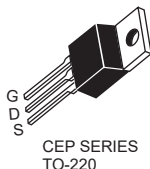
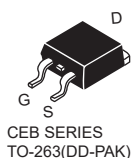
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

Type	$V_{DSS}@T_{Jmax}$	$R_{DS(ON)}$	I_D	@ V_{GS}
CEP38N65SF	700V	0.1 Ω	38A	10V
CEB38N65SF	700V	0.1 Ω	38A	10V
CEF38N65SF	700V	0.1 Ω	38A ^d	10V

- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	± 30		V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	38	38 ^d	A
		24	24 ^d	A
Drain Current-Pulsed ^a	I_{DM}^e	152	152 ^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	357	89	W
		2.9	0.7	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^g	E_{AS}	960		mJ
Single Pulsed Avalanche Current ^g	I_{AS}	8		A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.35	1.4	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	$^\circ\text{C}/\text{W}$

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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<http://www.cet-mos.com>



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			5	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.5		4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		0.084	0.1	Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 150V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		2225		pF
Output Capacitance	C_{oss}			115		pF
Reverse Transfer Capacitance	C_{rss}			5		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520V, I_D = 20A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		39		ns
Turn-On Rise Time	t_r			12		ns
Turn-Off Delay Time	$t_{d(off)}$			86		ns
Turn-Off Fall Time	t_f			8		ns
Total Gate Charge	Q_g	$V_{DS} = 520V, I_D = 20A,$ $V_{GS} = 10V$		67		nC
Gate-Source Charge	Q_{gs}			14		nC
Gate-Drain Charge	Q_{gd}			28		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				38	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.5	V
Reverse Recovery Time	T_{rr}	$I_F = 10A, di/dt = 100A/\mu s$		139.77		ns
Reverse Recovery Charge	Q_{rr}			0.8		μC
Peak Reverse Recovery Current	I_{rr}			10.73		A
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 19A$. g.L = 30mH, $I_{AS} = 8A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$.						



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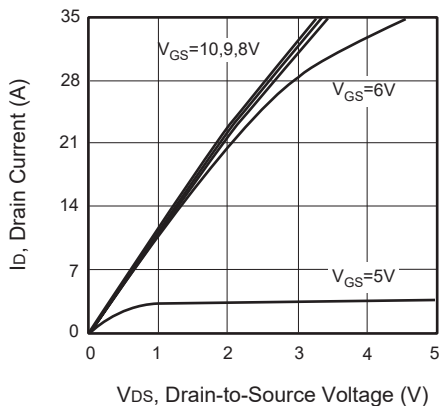


Figure 1. Output Characteristics

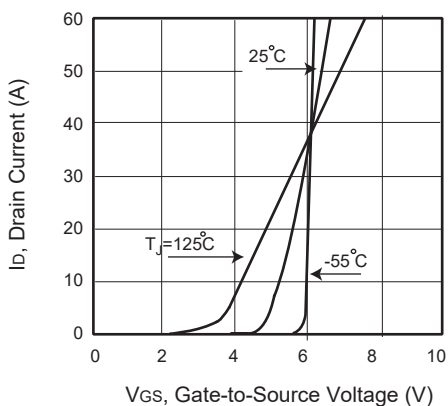


Figure 2. Transfer Characteristics

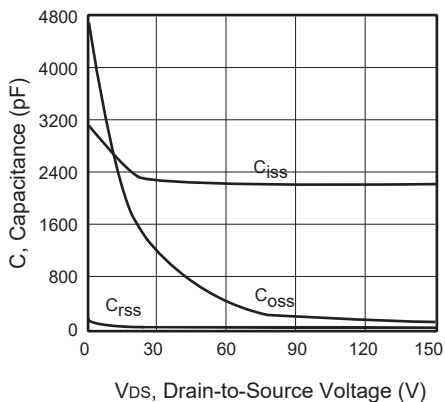


Figure 3. Capacitance

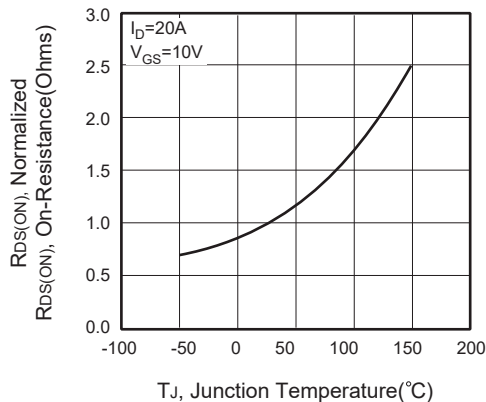


Figure 4. On-Resistance Variation with Temperature

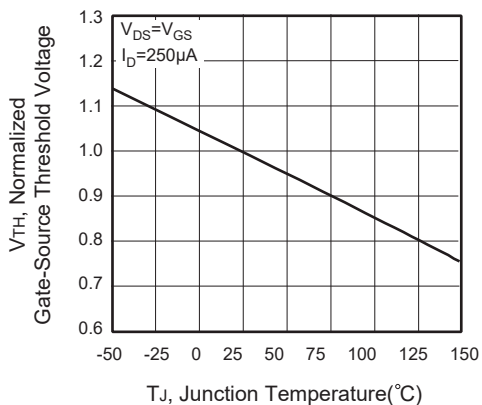


Figure 5. Gate Threshold Variation with Temperature

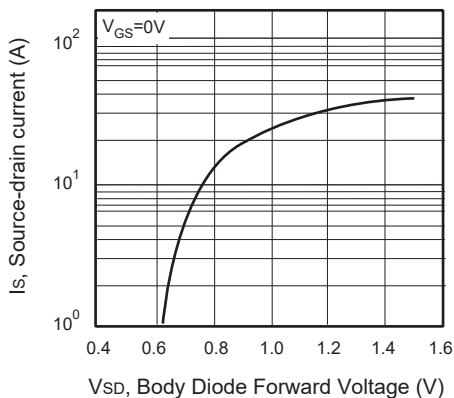


Figure 6. Body Diode Forward Voltage Variation with Source Current

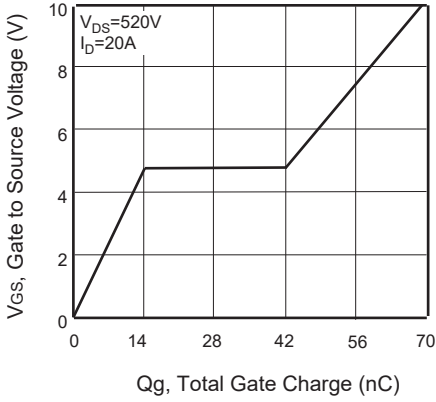


Figure 7. Gate Charge

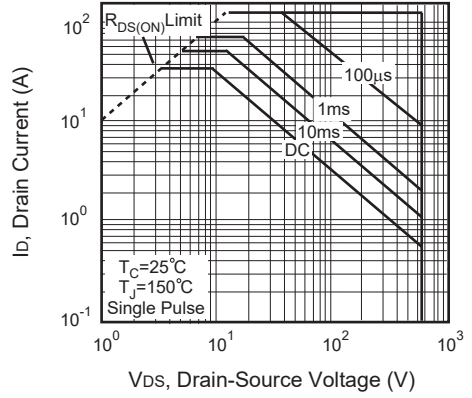


Figure 8. Maximum Safe Operating Area

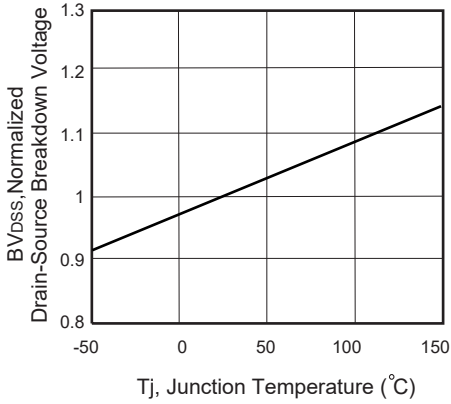


Figure 9. Breakdown Voltage Variation VS Temperature

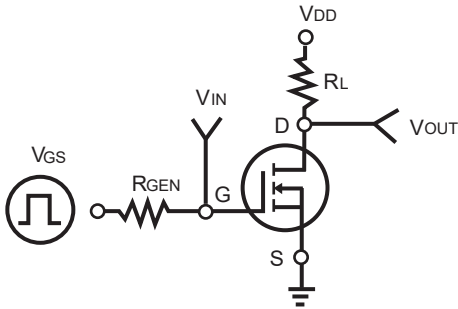


Figure 10. Switching Test Circuit

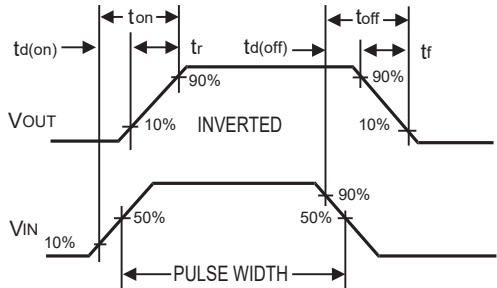


Figure 11. Switching Waveforms



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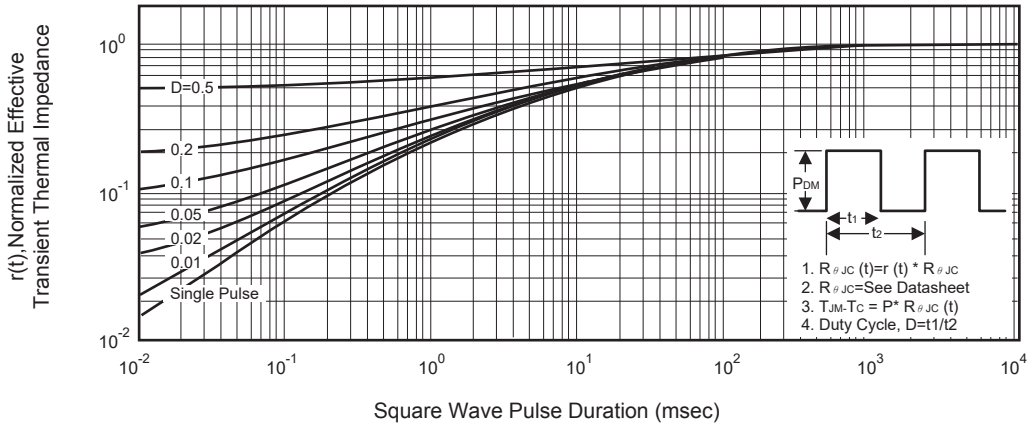


Figure 12. Normalized Thermal Transient Impedance Curve