



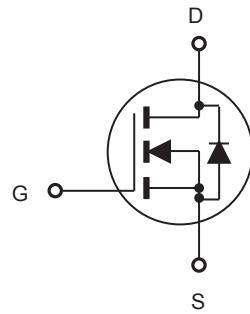
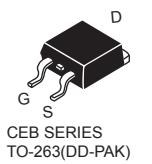
# CEP02N6G/CEB02N6G CEF02N6G

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP02N6G	600V	5Ω	2.2A	10V
CEB02N6G	600V	5Ω	2.2A	10V
CEF02N6G	600V	5Ω	2.2A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handing capability.
- Lead free product is acquired.



### ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	600		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	2.2 1.4	2.2 <sup>d</sup> 1.4 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	8.8	8.8 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	60 0.48	33 0.26	W W/°C
Single Pulsed Avalanche Energy <sup>g</sup>	E <sub>AS</sub>	11.25		mJ
Single Pulsed Avalanche Current <sup>g</sup>	I <sub>AS</sub>	1.5		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	2.1	3.8	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



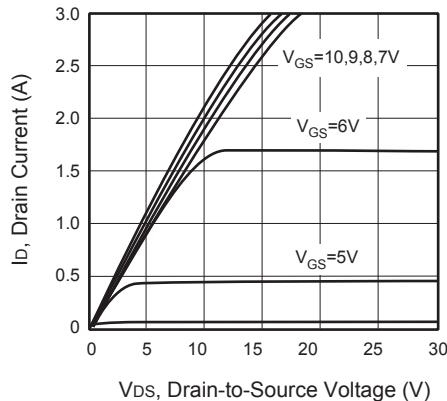
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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

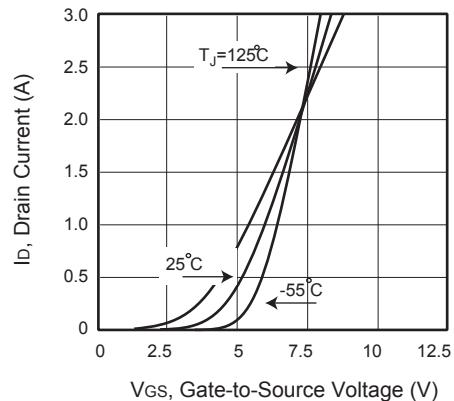
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	600			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 600\text{V}, V_{\text{GS}} = 0\text{V}$			25	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 30\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	2		4	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 1\text{A}$		3.8	5	$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		290		pF
Output Capacitance	$C_{\text{oss}}$			70		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 300\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 18\Omega$		18	36	ns
Turn-On Rise Time	$t_r$			10	20	ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			28	56	ns
Turn-Off Fall Time	$t_f$			10	20	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 480\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 10\text{V}$		6.8	9	nC
Gate-Source Charge	$Q_{\text{gs}}$			1.4		nC
Gate-Drain Charge	$Q_{\text{gd}}$			3.1		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$ <sup>f</sup>				2	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 1\text{A}$			1.5	V

**Notes :**

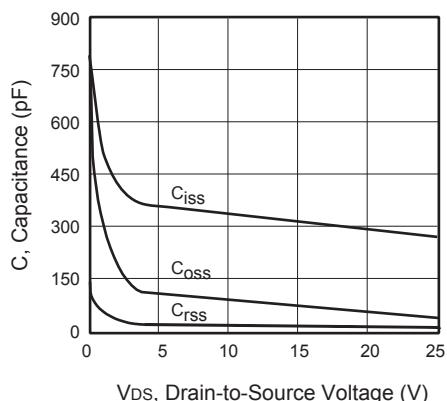
- a.Repetitive Rating : Pulse width limited by maximum junction temperature .
- b.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ . Duty Cycle  $\leq 2\%$  .  
c.Guaranteed by design, not subject to production testing.  
d.Limited only by maximum temperature allowed .  
e.Pulse width limited by safe operating area .  
f.Full package  $I_{\text{S}(\text{max})} = 1.5\text{A}$  .  
g.L = 10mH, IAS = 1.5A, VDD = 50V, RG = 25Ω, Starting TJ = 25 C



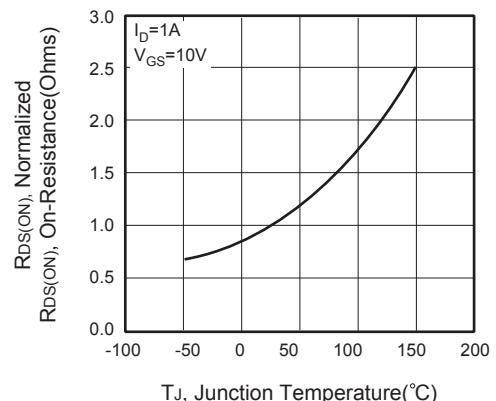
**Figure 1. Output Characteristics**



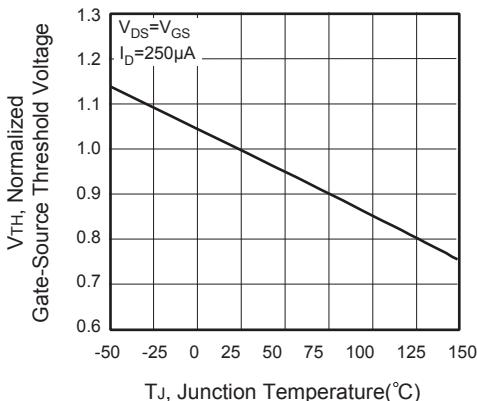
**Figure 2. Transfer Characteristics**



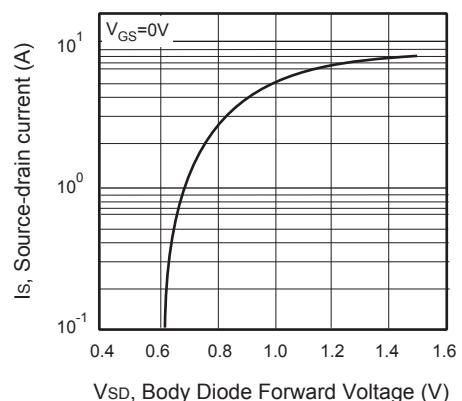
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**



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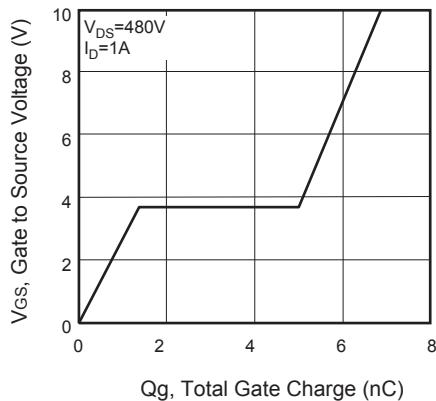


Figure 7. Gate Charge

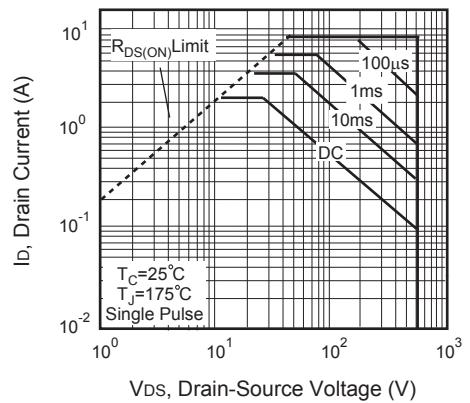


Figure 8. Maximum Safe Operating Area

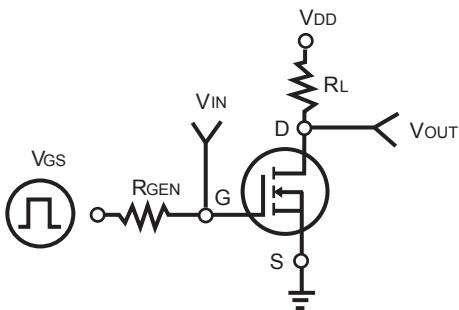


Figure 9. Switching Test Circuit

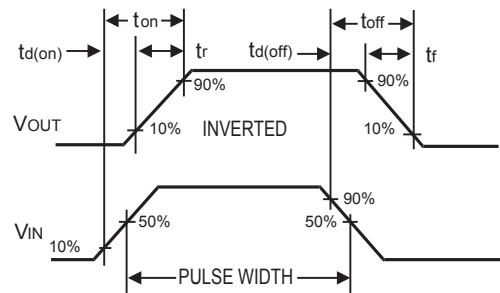


Figure 10. Switching Waveforms

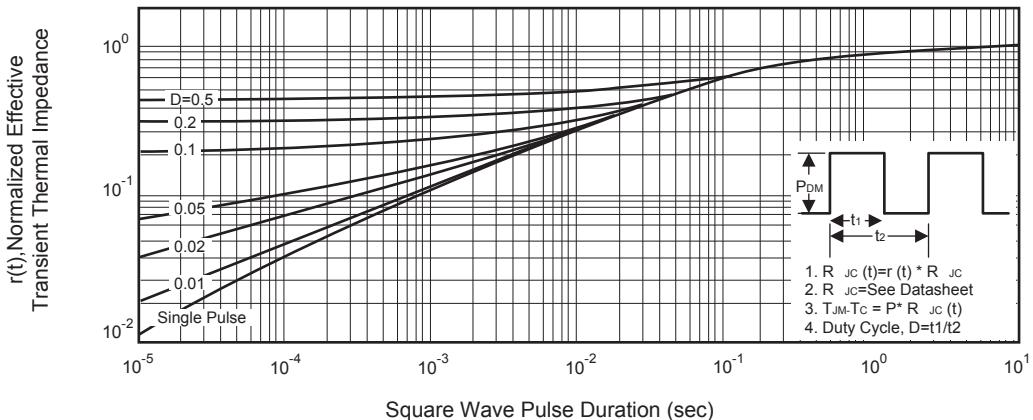


Figure 11. Normalized Thermal Transient Impedance Curve