

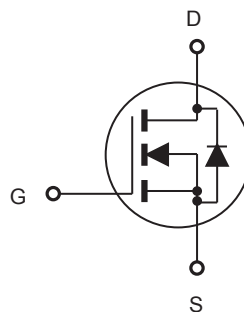
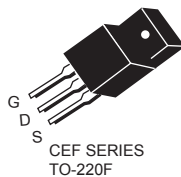
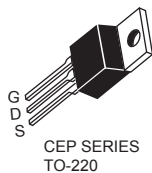
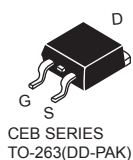
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

| Type | V _{DSS} | R _{DS(ON)} | I _D | @V _{GS} |
|---------|------------------|---------------------|------------------|------------------|
| CEP30N3 | 300V | 110mΩ | 30A | 10V |
| CEB30N3 | 300V | 110mΩ | 30A | 10V |
| CEF30N3 | 300V | 110mΩ | 30A ^e | 10V |

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Limit | | Units |
|--|-----------------------------------|------------|------------------|-------|
| | | TO-220/263 | TO-220F | |
| Drain-Source Voltage | V _{DS} | 300 | | V |
| Gate-Source Voltage | V _{GS} | ±30 | | V |
| Drain Current-Continuous | I _D | 30 | 30 ^e | A |
| Drain Current-Pulsed ^a | I _{DM} ^f | 120 | 120 ^e | A |
| Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C | P _D | 227 | 74 | W |
| | | 1.8 | 0.6 | W/°C |
| Single Pulsed Avalanche Energy ^d | E _{AS} | 450 | | mJ |
| Single Pulsed Avalanche Current ^d | I _{AS} | 30 | | A |
| Operating and Store Temperature Range | T _J , T _{stg} | -55 to 150 | | °C |

Thermal Characteristics

| Parameter | Symbol | Limit | | Units |
|---|------------------|-------|-----|-------|
| Thermal Resistance, Junction-to-Case | R _{θJC} | 0.55 | 1.7 | °C/W |
| Thermal Resistance, Junction-to-Ambient | R _{θJA} | 62.5 | 65 | °C/W |



CEP30N3/CEB30N3 CEF30N3

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|--------------|---|-----|------|------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = 250\mu A$ | 300 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 300V, V_{GS} = 0V$ | | | 1 | μA |
| Gate Body Leakage Current, Forward | I_{GSSF} | $V_{GS} = 30V, V_{DS} = 0V$ | | | 100 | nA |
| Gate Body Leakage Current, Reverse | I_{GSSR} | $V_{GS} = -30V, V_{DS} = 0V$ | | | -100 | nA |
| On Characteristics^b | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS} = V_{DS}, I_D = 250\mu A$ | 2 | | 4 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS} = 10V, I_D = 15A$ | | 85 | 110 | m Ω |
| Dynamic Characteristics^c | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$ | | 2800 | | pF |
| Output Capacitance | C_{oss} | | | 390 | | pF |
| Reverse Transfer Capacitance | C_{rss} | | | 5 | | pF |
| Switching Characteristics^c | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 150V, I_D = 32A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$ | | 40 | | ns |
| Turn-On Rise Time | t_r | | | 23 | | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 140 | | ns |
| Turn-Off Fall Time | t_f | | | 20 | | ns |
| Total Gate Charge | Q_g | $V_{DS} = 240V, I_D = 32A,$ $V_{GS} = 10V$ | | 64 | | nC |
| Gate-Source Charge | Q_{gs} | | | 18 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 22 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| Drain-Source Diode Forward Current | I_S^g | | | | 30 | A |
| Drain-Source Diode Forward Voltage ^b | V_{SD} | $V_{GS} = 0V, I_S = 30A^h$ | | | 1.5 | V |
| Notes : □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. □ c.Guaranteed by design, not subject to production testing. □ d.L = 1mH, $I_{AS} = 30A$, $V_{OD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25\text{ C}^\circ$. e.Limited only by maximum temperature allowed . f.Pulse width limited by safe operating area . g.Full package $I_{S(max)} = 17A$. h.Full package V_{SD} test condition $I_S = 17A$. | | | | | | |

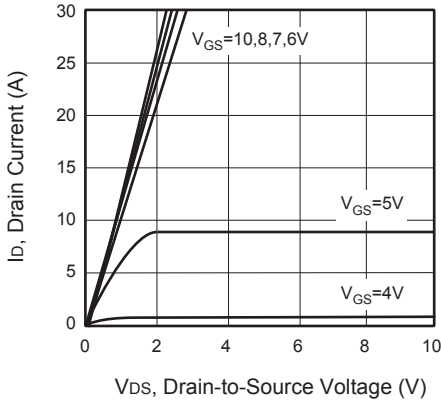


Figure 1. Output Characteristics

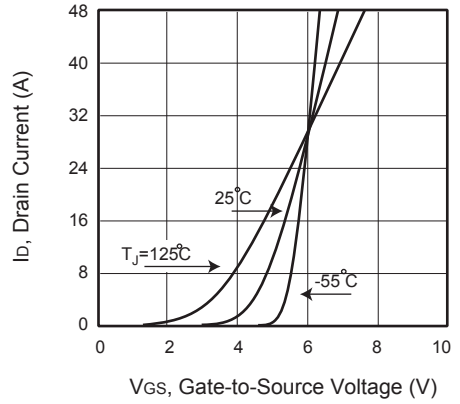


Figure 2. Transfer Characteristics

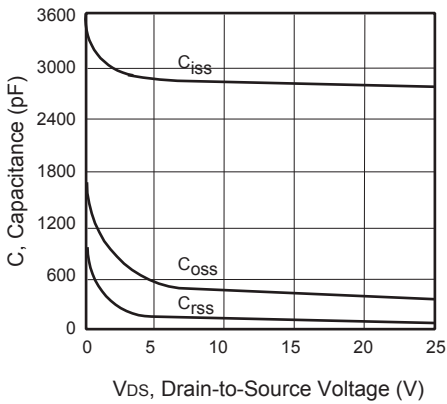


Figure 3. Capacitance

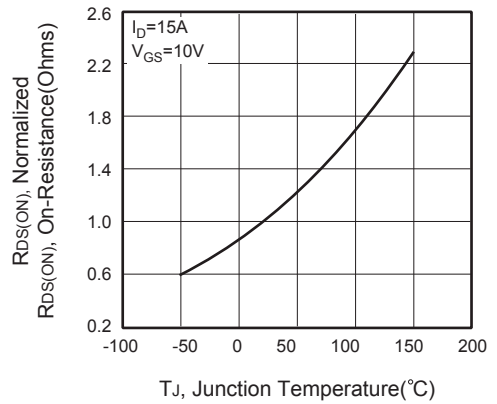


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

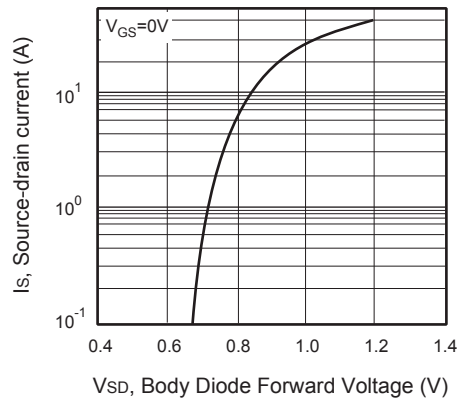


Figure 6. Body Diode Forward Voltage Variation with Source Current

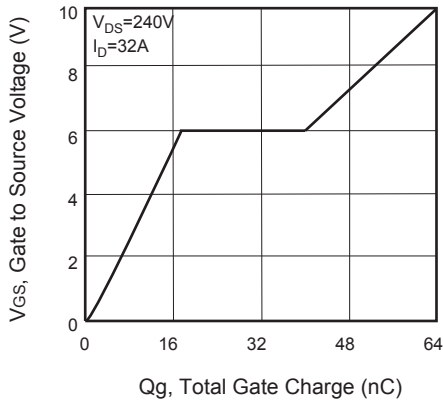


Figure 7. Gate Charge

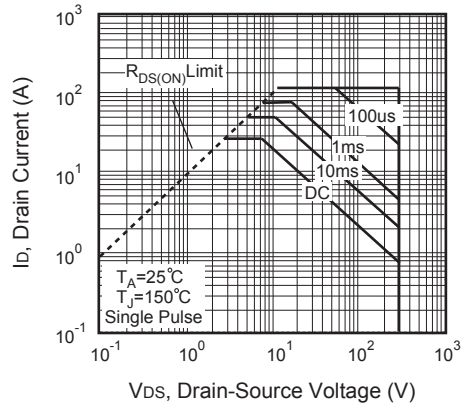


Figure 8. Maximum Safe Operating Area

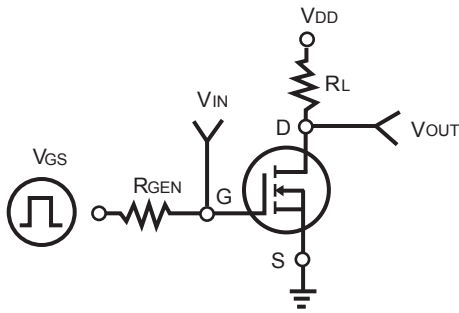


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

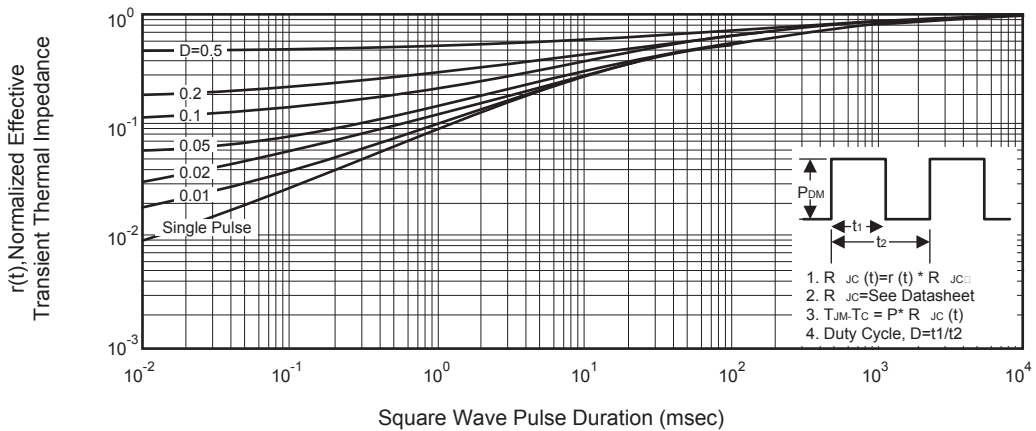


Figure 11. Normalized Thermal Transient Impedance Curve