



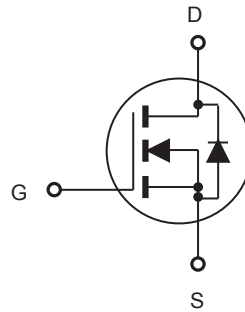
# CEPF634/CEBF634 CEIF634/CEFF634

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEPF634	250V	0.45Ω	8.1A	10V
CEBF634	250V	0.45Ω	8.1A	10V
CEIF634	250V	0.45Ω	8.1A	10V
CEFF634	250V	0.45Ω	8.1A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	250		V
Gate-Source Voltage	V <sub>GS</sub>	±20		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	8.1	8.1 <sup>d</sup>	A
		5.1	5.1 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	32	32 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	74	38	W
		0.59	0.3	W/°C
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.7	3.3	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	250			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250V, V_{GS} = 0V$			25	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4.5A$			0.45	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 50V, I_D = 5.1A$		4.4		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		925		pF
Output Capacitance	$C_{oss}$			95		pF
Reverse Transfer Capacitance	$C_{rss}$			20		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125V, I_D = 5.6A, V_{GS} = 10V, R_{GEN} = 12\Omega$		16	32	ns
Turn-On Rise Time	$t_r$			3.5	7	ns
Turn-Off Delay Time	$t_{d(off)}$			38	76	ns
Turn-Off Fall Time	$t_f$			4	8	ns
Total Gate Charge	$Q_g$	$V_{DS} = 200V, I_D = 5.6A, V_{GS} = 10V$		18	23	nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			5		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				8.1	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 8.1A$		0.9	1.5	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . □ c.Guaranteed by design, not subject to production testing. □ d.Limited only by maximum temperature allowed . e .Pulse width limited by safe operating area . f .Full package $I_{S(max)} = 6A$ . g .UIS condition $V_{dd}=25V$ $L=2mH$ $R_g=25ohm$ $I_{as}=8.1A$ .						

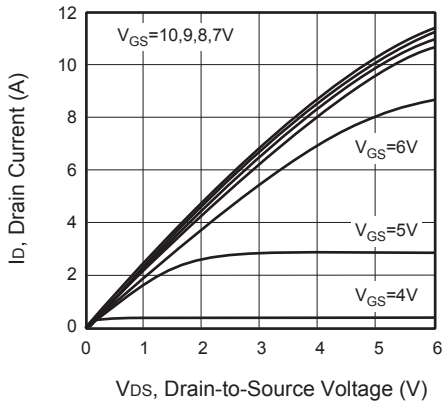


Figure 1. Output Characteristics

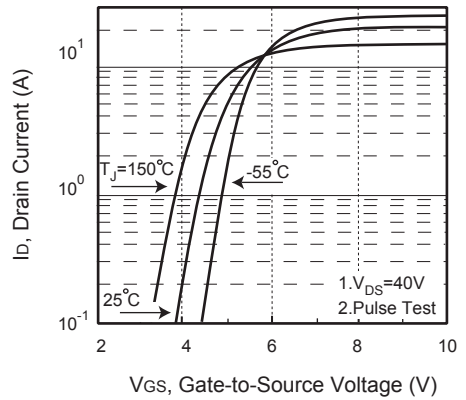


Figure 2. Transfer Characteristics

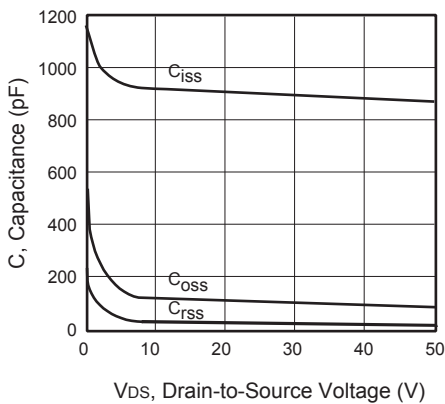


Figure 3. Capacitance

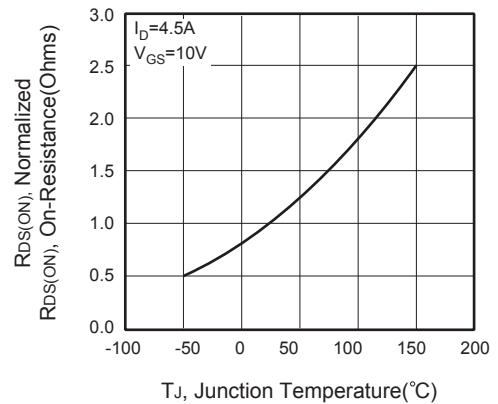


Figure 4. On-Resistance Variation with Temperature

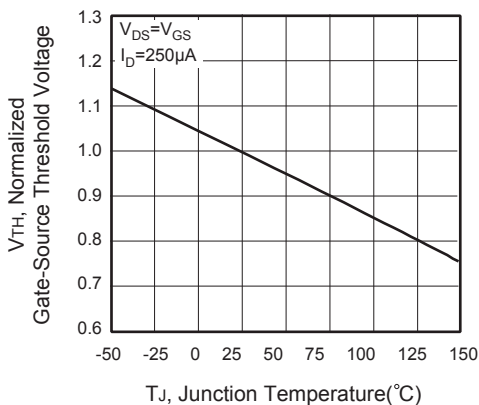


Figure 5. Gate Threshold Variation with Temperature

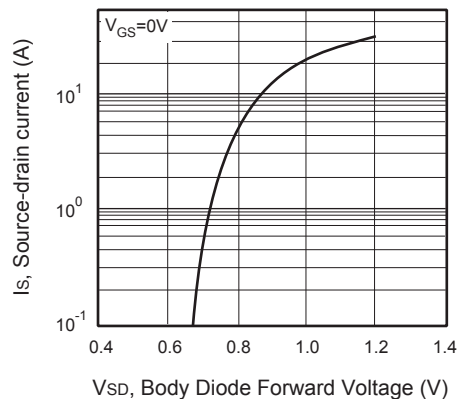


Figure 6. Body Diode Forward Voltage Variation with Source Current

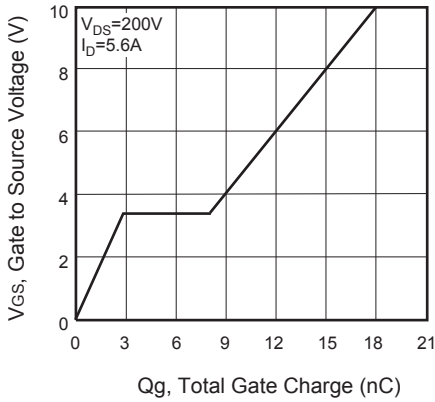


Figure 7. Gate Charge

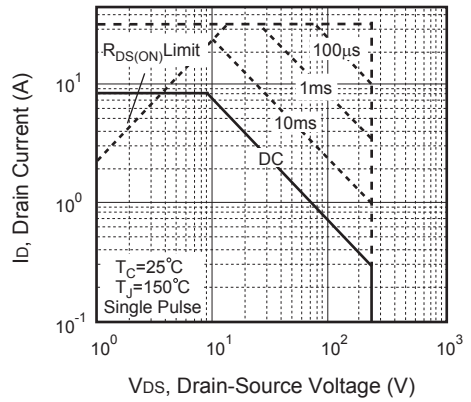


Figure 8. Maximum Safe Operating Area

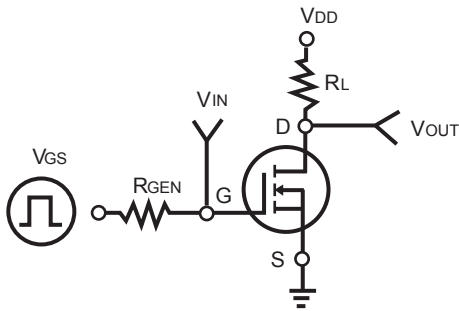


Figure 9. Switching Test Circuit

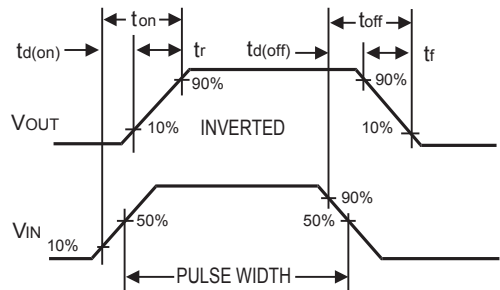


Figure 10. Switching Waveforms

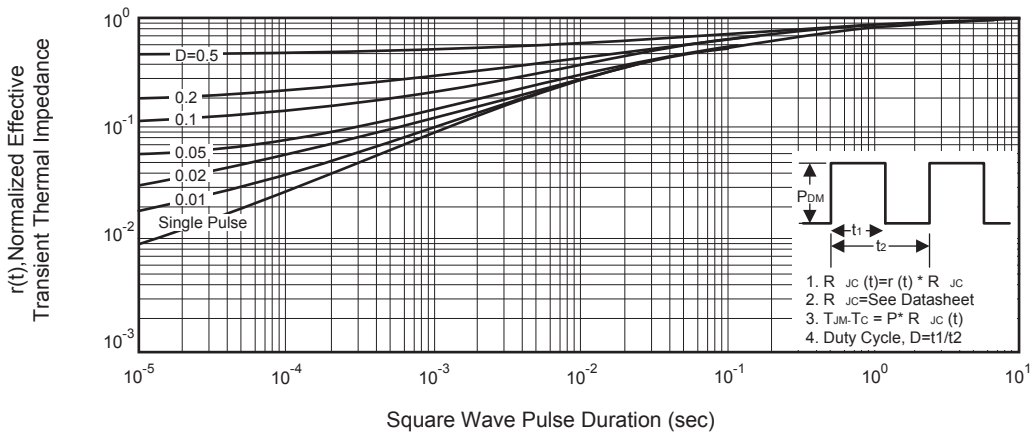


Figure 11. Normalized Thermal Transient Impedance Curve