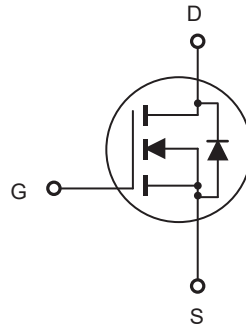


## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 100V, 36A,  $R_{DS(ON)} = 16.5m\Omega @V_{GS} = 10V$ .  
 $R_{DS(ON)} = 24 m\Omega @V_{GS} = 4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- RoHS compliant.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$I_D$	36	A
		22	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	144	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	35.7	W
		0.28	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	10	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	4.5	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$



# CED1610LA/CEU1610LA

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		13.4	16.5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$		18	24	$m\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		900		pF
Output Capacitance	$C_{oss}$			205		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 1A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		17		ns
Turn-On Rise Time	$t_r$			4		ns
Turn-Off Delay Time	$t_{d(off)}$			42		ns
Turn-Off Fall Time	$t_f$			20		ns
Total Gate Charge	$Q_g$	$V_{DS} = 50V, I_D = 20A,$ $V_{GS} = 4.5V$		11.5		nC
Gate-Source Charge	$Q_{gs}$			1.7		nC
Gate-Drain Charge	$Q_{gd}$			7.8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				29	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 20A$			1.2	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width < 300 $\mu s$ , Duty Cycle < 2%. c.Guaranteed by design, not subject to production testing. d. L=1mH, $I_{AS}=4.5A$ , $V_{DD}=24V$ , $R_G=25\Omega$ , Starting $T_J=25^\circ\text{C}$ .						

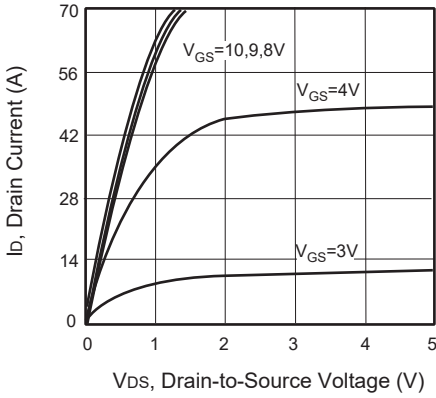


Figure 1. Output Characteristics

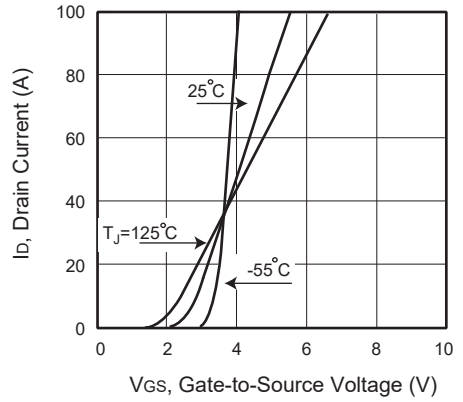


Figure 2. Transfer Characteristics

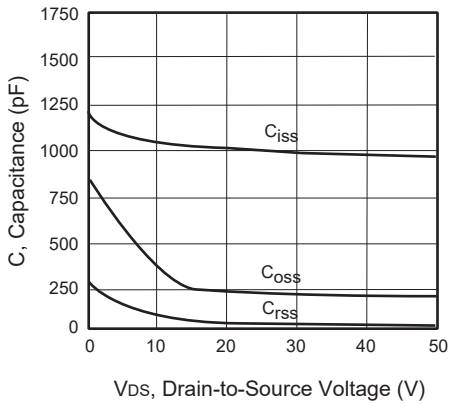


Figure 3. Capacitance

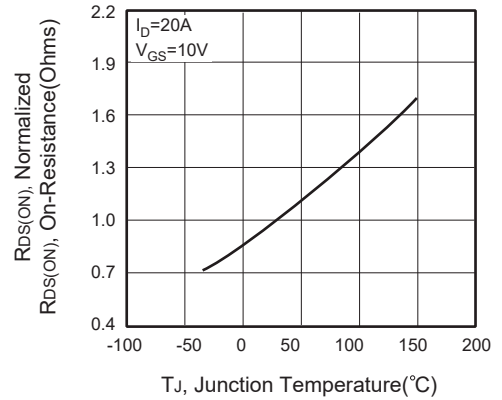


Figure 4. On-Resistance Variation with Temperature

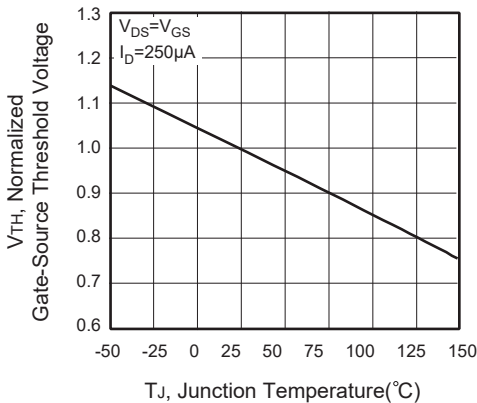


Figure 5. Gate Threshold Variation with Temperature

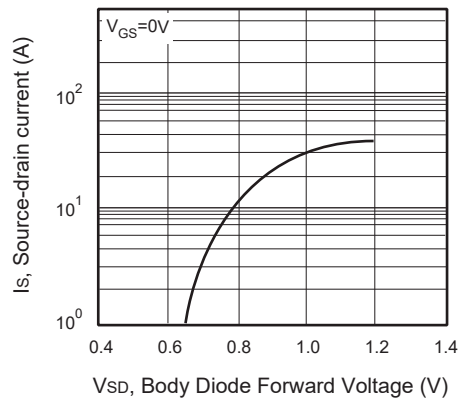
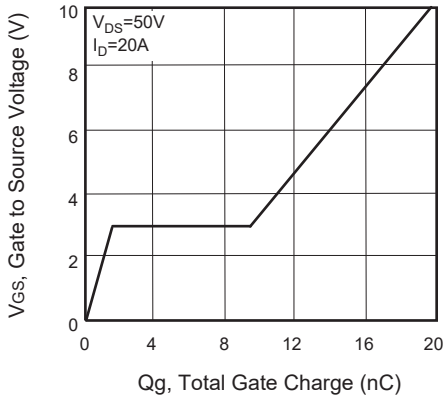
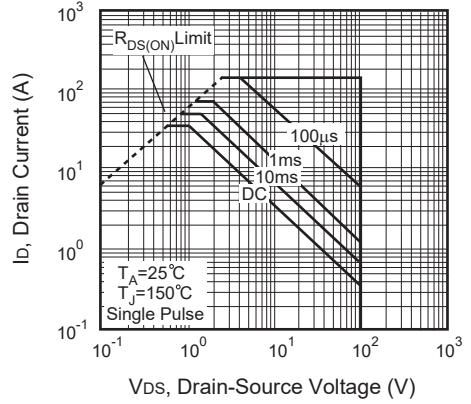


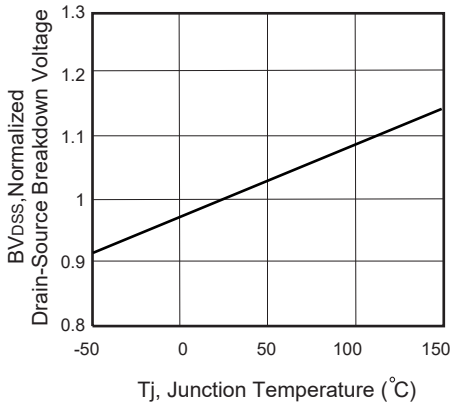
Figure 6. Body Diode Forward Voltage Variation with Source Current



**Figure 7. Gate Charge**



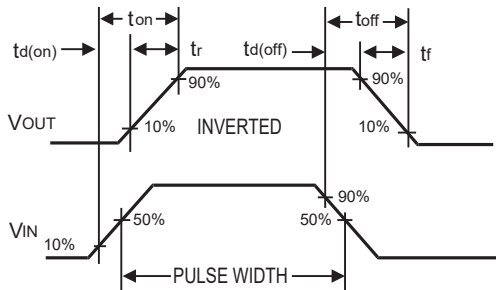
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**

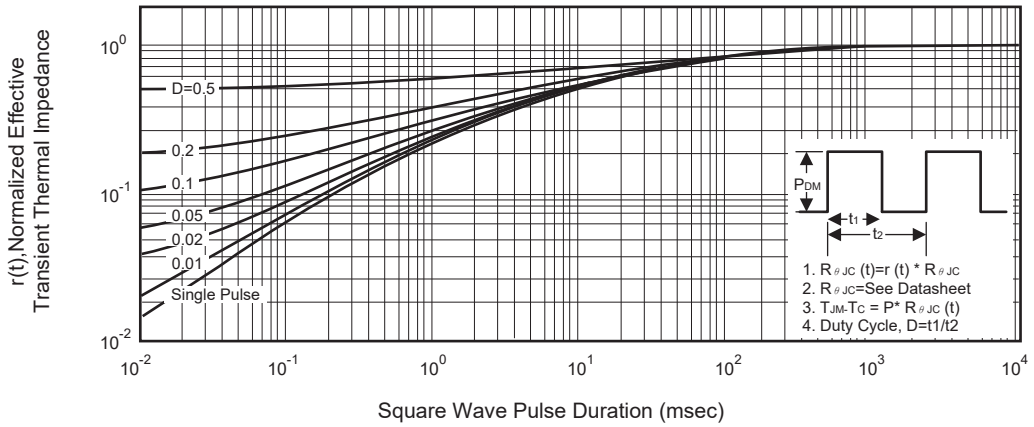


Figure 12. Normalized Thermal Transient Impedance Curve