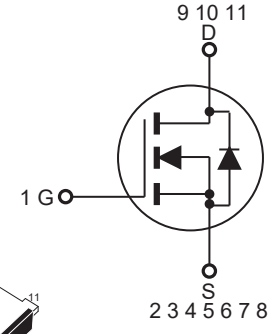
CEL39100

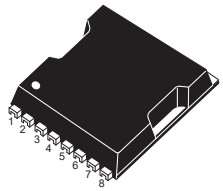
N-Channel Enhancement Mode Field Effect Transistor

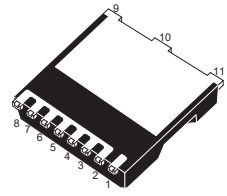
PRELIMINARY

FEATURES

- 100V , 385A, $R_{DS(ON)}$ = 1.4mΩ @V_{GS} = 10V
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.
- TOLL package.







Applications

- Battery management.
- Load swith.
- Solar.

ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous@ T_C = 25°C	I_D	385	A
@ T_C = 100°C		272	A
Drain Current-Pulsed [a]	I_{DM}	1540	A
Maximum Power Dissipation @ T_C = 25°C	P_D	417	W
- Derate above 25°C		2.8	W/°C
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.36	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	°C/W

This is preliminary information on a new product in development now
Details are subject to change without notice .

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http://www.cet-mos.com

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A		1.1	1.4	mΩ
		V_{GS} = 4.5V, I_D = 20A		1.8	2.3	mΩ
Gate input resistance	R_g	f=1MHz,open Drain		2		Ω
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 50V, V_{GS} = 0V, f = 1.0 MHz		14070		pF
Output Capacitance	C_{oss}			1830		pF
Reverse Transfer Capacitance	C_{rss}			245		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 20A, V_{GS} =10V, R_{GEN} = 6Ω		43		ns
Turn-On Rise Time	t_r			39		ns
Turn-Off Delay Time	$t_{d(off)}$			184		ns
Turn-Off Fall Time	t_f			117		ns
Total Gate Charge	Q_g	V_{DS} = 50V, I_D = 20A, V_{GS} = 10V		191		nC
Gate-Source Charge	Q_{gs}			26		nC
Gate-Drain Charge	Q_{gd}			64		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				347	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 20A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

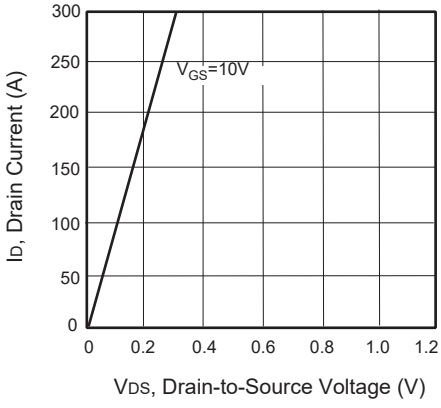


Figure 1. Output Characteristics

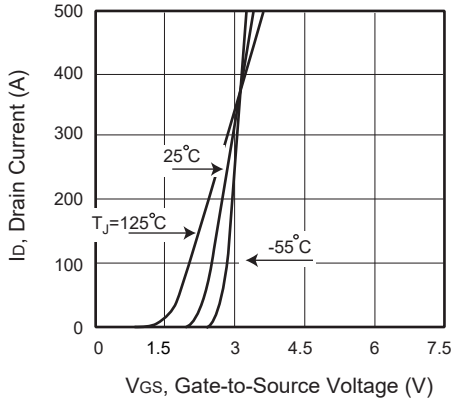


Figure 2. Transfer Characteristics

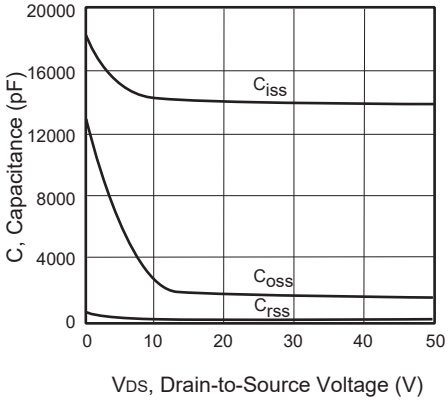


Figure 3. Capacitance

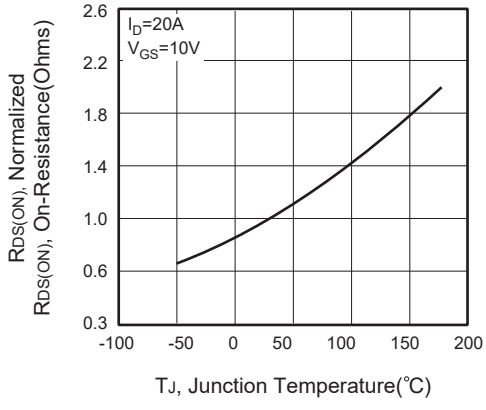


Figure 4. On-Resistance Variation with Temperature

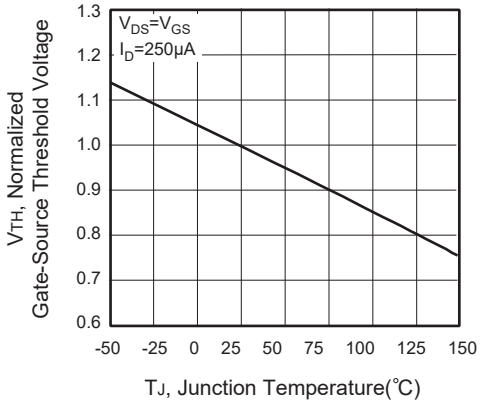


Figure 5. Gate Threshold Variation with Temperature

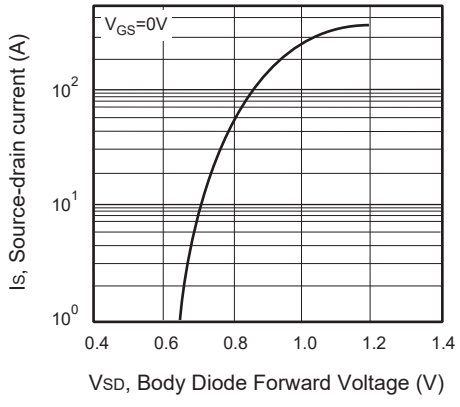


Figure 6. Body Diode Forward Voltage Variation with Source Current

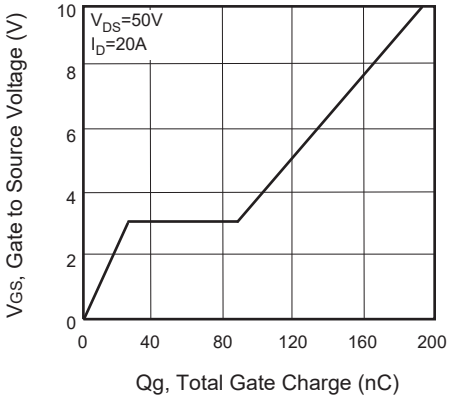


Figure 7. Gate Charge

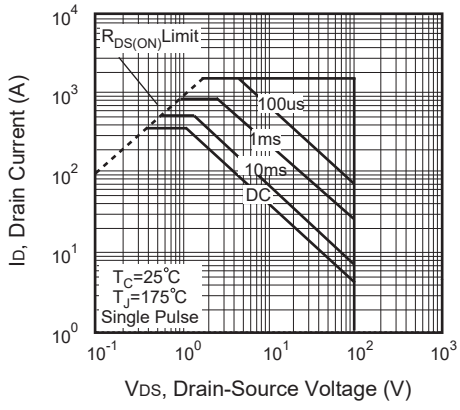


Figure 8. Maximum Safe Operating Area

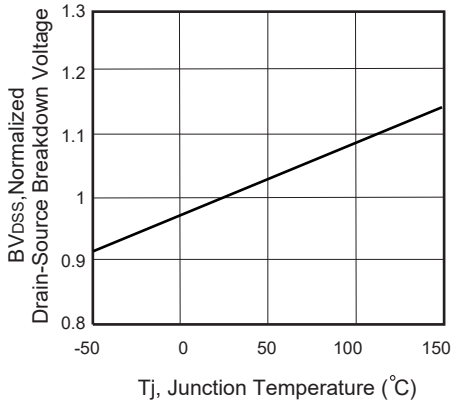


Figure 9. Breakdown Voltage Variation VS Temperature

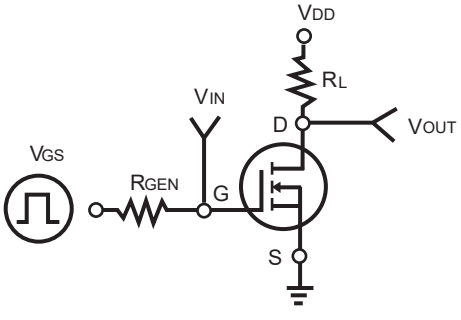


Figure 10. Switching Test Circuit

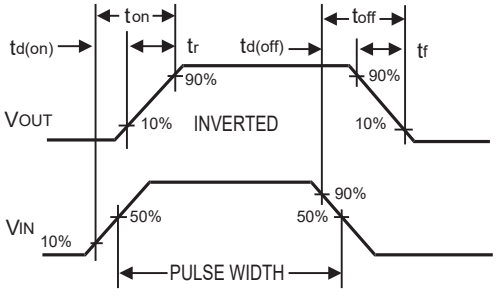


Figure 11. Switching Waveforms

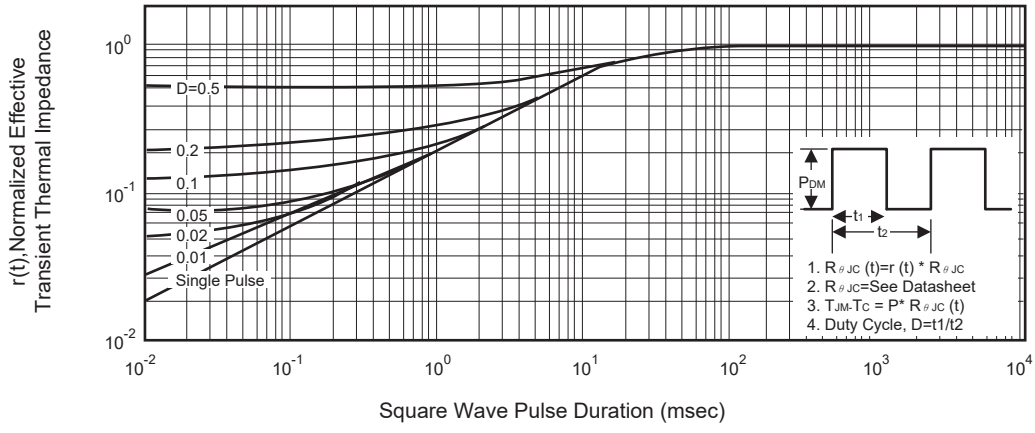
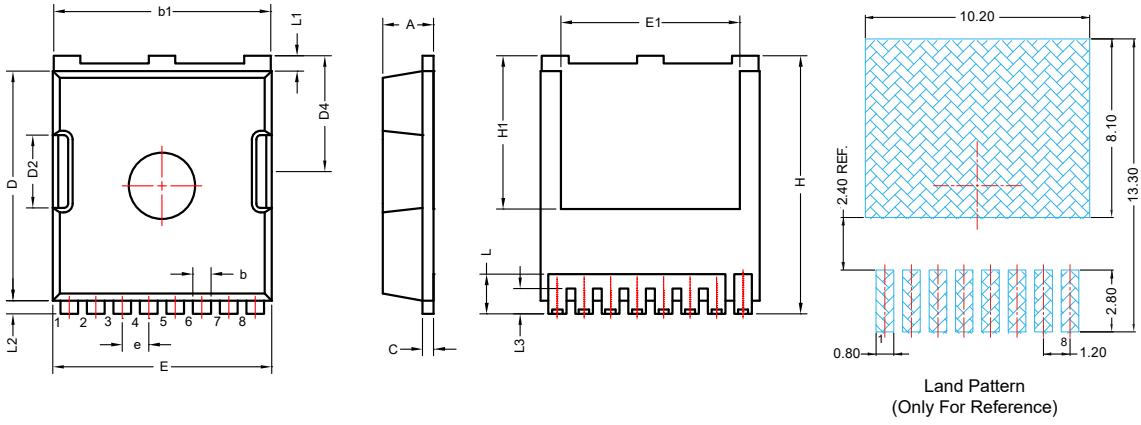


Figure 12. Normalized Thermal Transient Impedance Curve

TOLL 產品外觀尺寸圖 (Product Outline Dimension)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.150	2.450	0.085	0.096
b	0.700	0.900	0.028	0.035
b1	9.650	9.950	0.380	0.392
c	0.400	0.600	0.016	0.024
D	10.180	10.580	0.401	0.417
D2	3.150	3.450	0.124	0.136
D4	4.400	4.700	0.173	0.185
E	9.700	10.100	0.382	0.398
E1	7.950	8.250	0.313	0.325
e	1.20BSC		0.047BSC	
H	11.480	11.880	0.452	0.468
H1	6.800	7.100	0.268	0.280
L	1.500	2.100	0.059	0.083
L1	0.500	0.900	0.020	0.035
L2	0.500	0.720	0.020	0.028
L3	1.000	1.300	0.039	0.051