CEH2609A

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

■ 20V, 4A, $R_{DS(ON)}$ = 45mΩ @V_{GS} = 4.5V.
$R_{DS(ON)}$ = 55mΩ @V_{GS} = 2.5V.

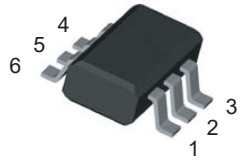
■ -20V, -2.8A, $R_{DS(ON)}$ = 90mΩ @V_{GS} = -4.5V.
$R_{DS(ON)}$ = 120mΩ @V_{GS} = -2.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

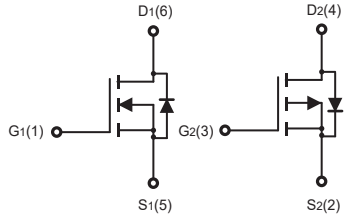
■ High power and current handing capability.

■ RoHS compliant.

■ Surface mount Package.



TSOP-6



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±12	±12	V
Drain Current-Continuous	I_D	4	-2.8	A
Drain Current-Pulsed [a]	I_{DM}	16	-11.2	A
Maximum Power Dissipation	P_D	1.14		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	110	°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	0.4		1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3.5A		32	45	mΩ
		V_{GS} = 2.5V, I_D = 2A		39	55	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f = 1.0 MHz		470		pF
Output Capacitance	C_{oss}			85		pF
Reverse Transfer Capacitance	C_{rss}			50		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 4A, V_{GS} = 4.5V, R_{GEN} = 6Ω		10		ns
Turn-On Rise Time	t_r			5		ns
Turn-Off Delay Time	$t_{d(off)}$			36		ns
Turn-Off Fall Time	t_f			9		ns
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 4A, V_{GS} = 4.5V		4.7		nC
Gate-Source Charge	Q_{gs}			0.4		nC
Gate-Drain Charge	Q_{gd}			1.2		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1.14	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1A			1.1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-CHANNEL Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-0.4		-1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.5A		66	90	mΩ
		V_{GS} = -2.5V, I_D = -1.5A		82	120	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -10V, V_{GS} = 0V, f = 1.0 MHz		515		pF
Output Capacitance	C_{oss}			75		pF
Reverse Transfer Capacitance	C_{rss}			50		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GEN} = 3Ω		12		ns
Turn-On Rise Time	t_r			5		ns
Turn-Off Delay Time	$t_{d(off)}$			81		ns
Turn-Off Fall Time	t_f			34		ns
Total Gate Charge	Q_g	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V		5.8		nC
Gate-Source Charge	Q_{gs}			0.5		nC
Gate-Drain Charge	Q_{gd}			1.6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-1.14	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t < 5 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

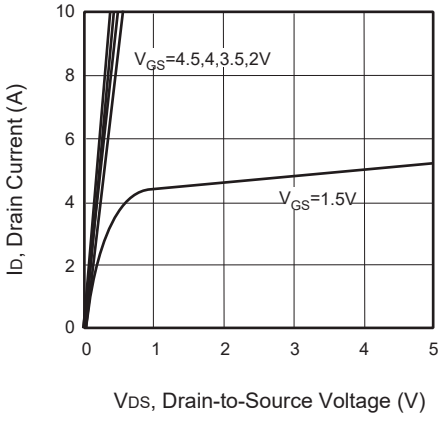


Figure 1. Output Characteristics

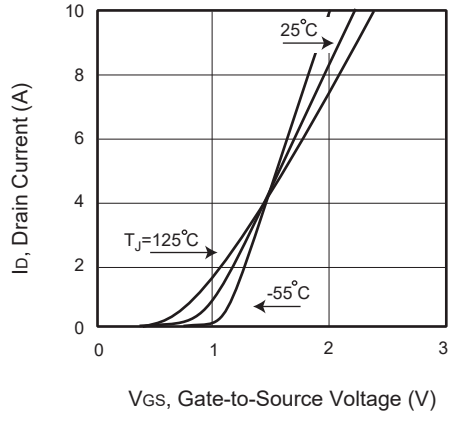


Figure 2. Transfer Characteristics

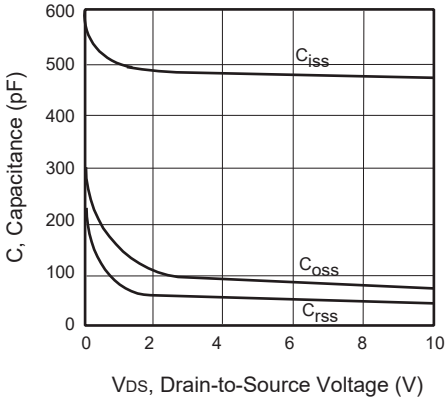


Figure 3. Capacitance

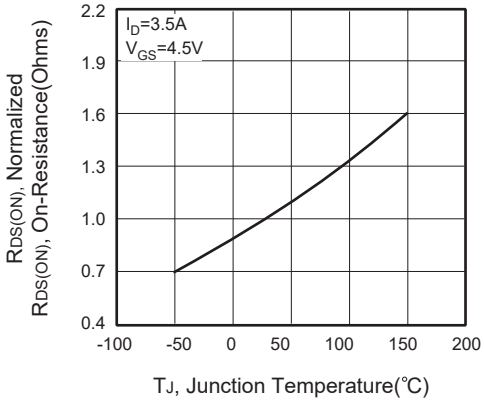


Figure 4. On-Resistance Variation with Temperature

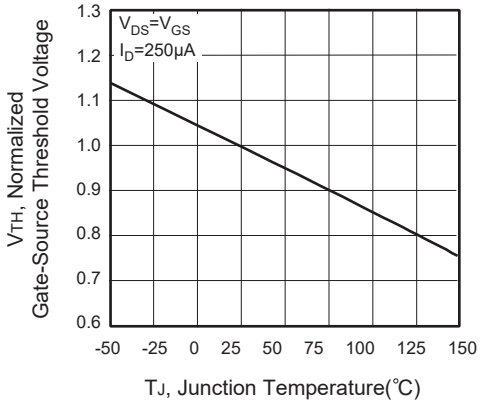


Figure 5. Gate Threshold Variation with Temperature

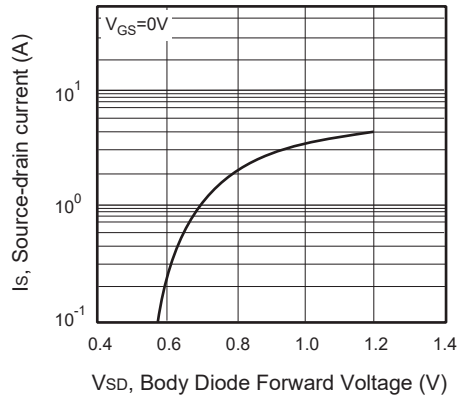


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

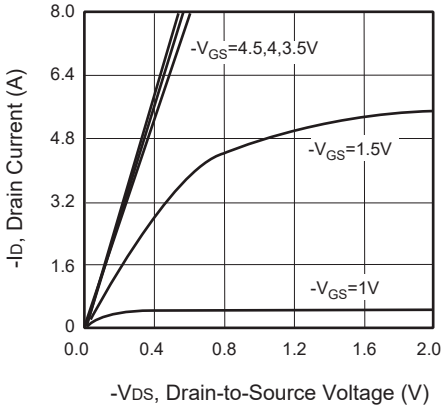


Figure 7. Output Characteristics

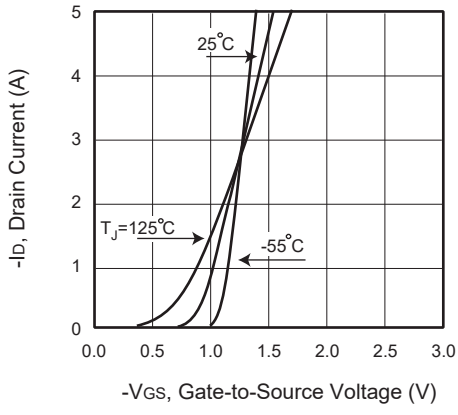


Figure 8. Transfer Characteristics

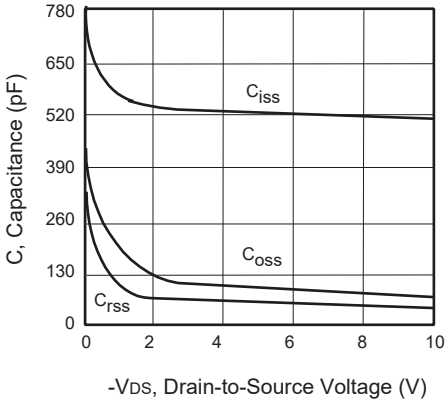


Figure 9. Capacitance

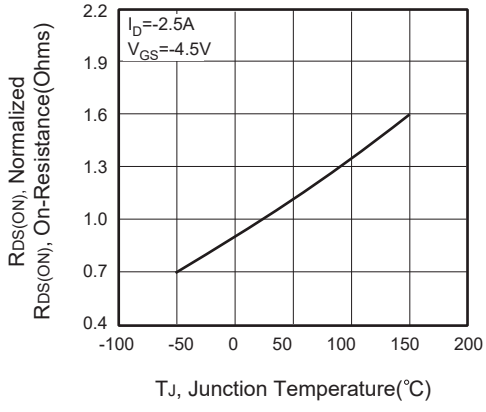


Figure 10. On-Resistance Variation with Temperature

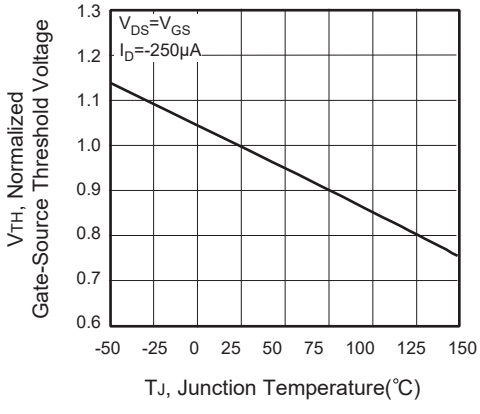


Figure 11. Gate Threshold Variation with Temperature

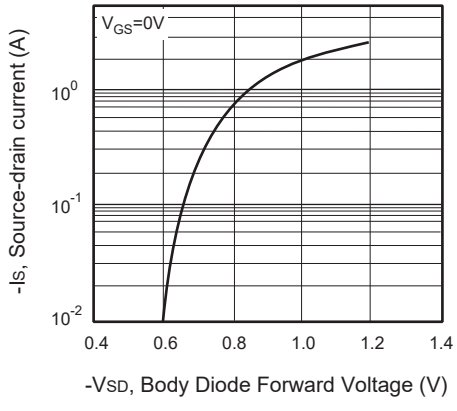


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

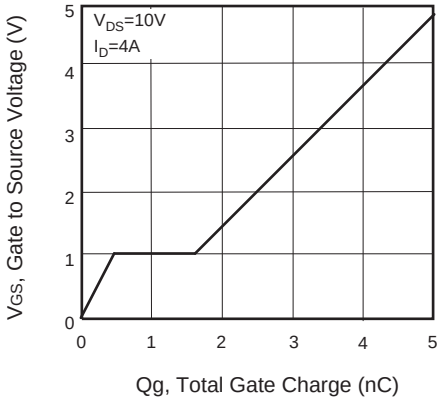


Figure 13. Gate Charge

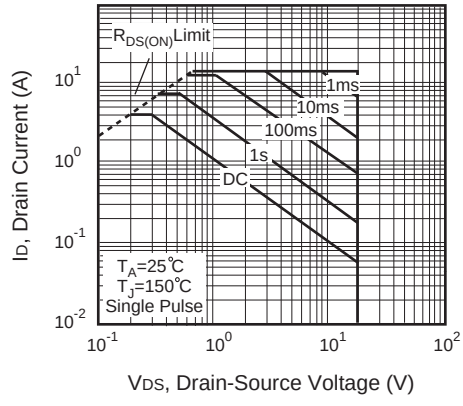


Figure 14. Maximum Safe Operating Area

P-CHANNEL

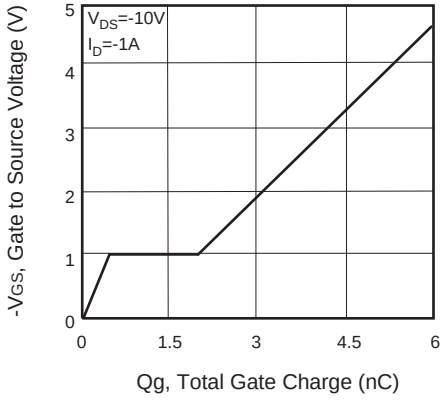


Figure 15. Gate Charge

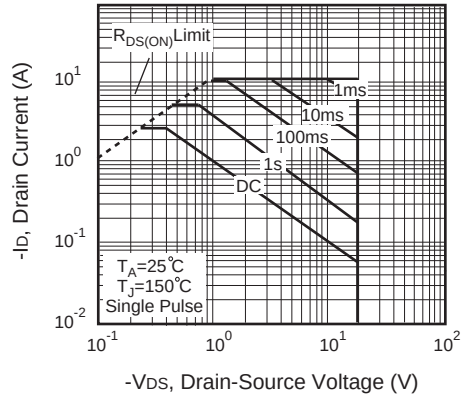


Figure 16. Maximum Safe Operating Area

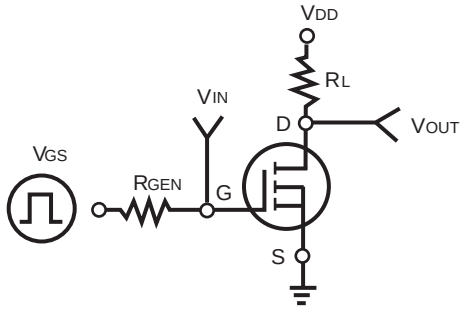


Figure 17. Switching Test Circuit

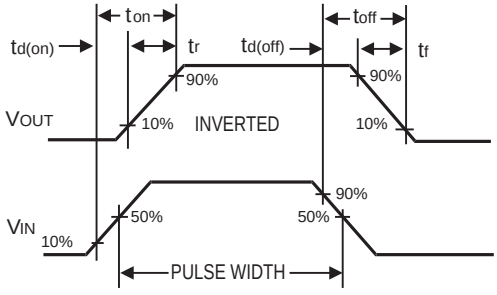


Figure 18. Switching Waveforms

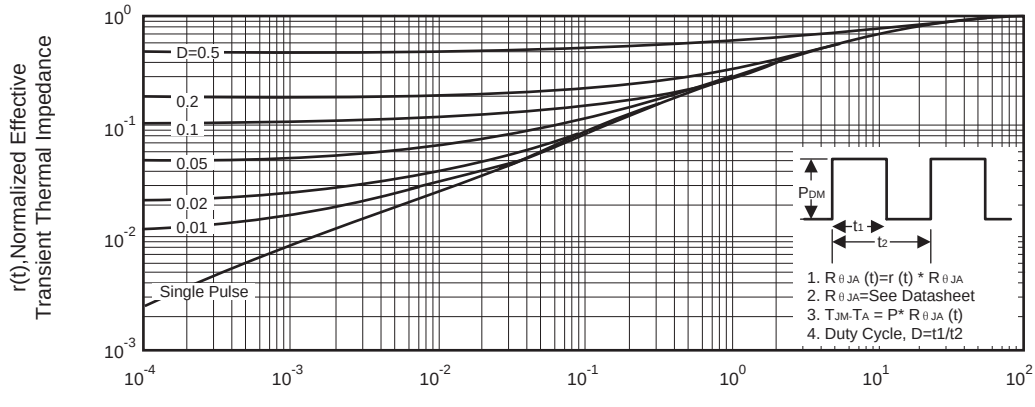


Figure 19. Normalized Thermal Transient Impedance Curve