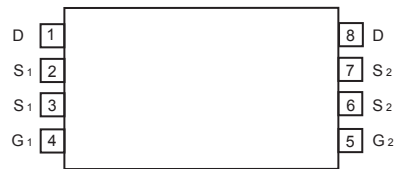
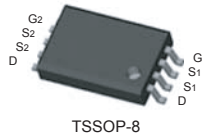
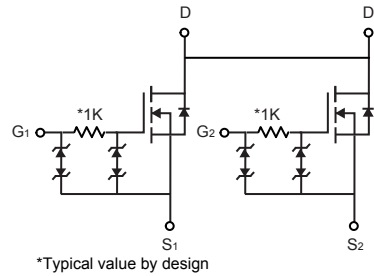


## Dual N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 20V, 6.5A,  $R_{DS(ON)} = 22m\Omega @ V_{GS} = 4.5V$ .  
 $R_{DS(ON)} = 32m\Omega @ V_{GS} = 2.5V$ .
- Super High dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TSSOP-8 for Surface Mount Package.
- ESD Protected: HBM 2000 V



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

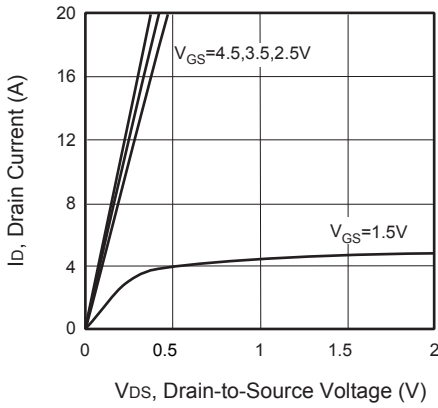
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	6.5	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	25	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

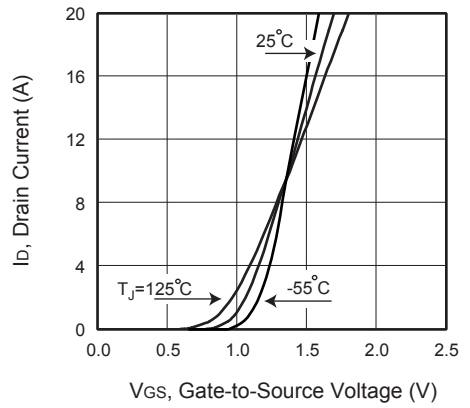
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	83	$^\circ C/W$

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

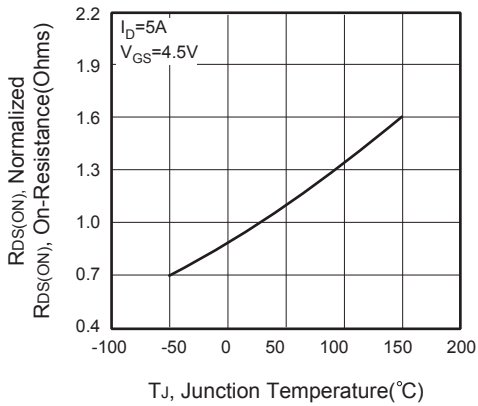
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 12V, V_{DS} = 0V$			10	$\mu A$
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -12V, V_{DS} = 0V$			-10	$\mu A$
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	0.5		1.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 5A$		18	22	$m\Omega$
		$V_{GS} = 2.5V, I_D = 4A$		24	32	$m\Omega$
<b>Dynamic Characteristics <sup>c</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 5A$		17		S
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		40		pF
Output Capacitance	$C_{oss}$			115		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics <sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GEN} = 6\Omega$		0.35	0.7	$\mu s$
Turn-On Rise Time	$t_r$			0.87	1.8	$\mu s$
Turn-Off Delay Time	$t_{d(off)}$			3.60	7.5	$\mu s$
Turn-Off Fall Time	$t_f$			2.01	4.3	$\mu s$
Total Gate Charge	$Q_g$	$V_{DS} = 10V, I_D = 5A, V_{GS} = 4.5V$		4.3	7.5	nC
Gate-Source Charge	$Q_{gs}$			1.1		nC
Gate-Drain Charge	$Q_{gd}$			2.5		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				1.5	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 1.5A$			1.2	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 board, $t \leq 10\text{sec}$ . □ b.Pulse Test : Pulse Width < 300 $\mu s$ , Duty Cycle < 2%. □ c.Guaranteed by design, not subject to production testing. □						



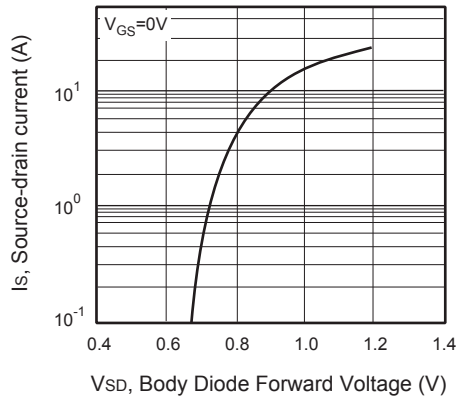
**Figure 1. Output Characteristics**



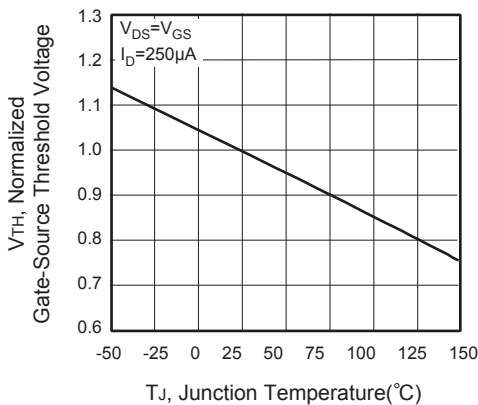
**Figure 2. Transfer Characteristics**



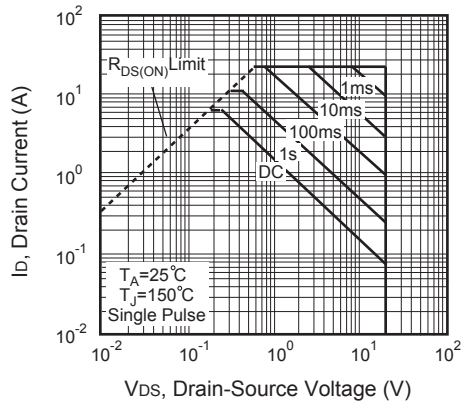
**Figure 3. On-Resistance Variation with Temperature**



**Figure 4. Body Diode Forward Voltage Variation with Source Current**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Maximum Safe Operating Area**

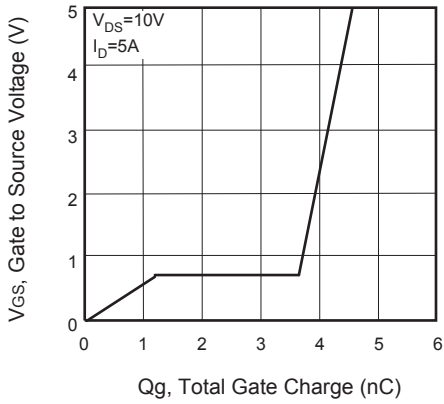


Figure 7. Gate Charge

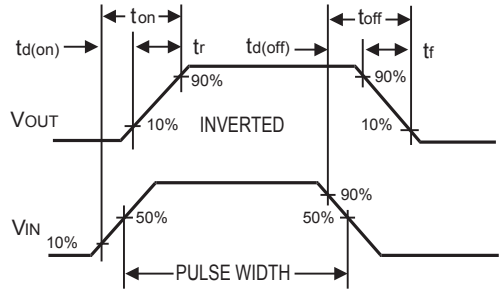


Figure 8. Switching Waveforms



Figure 9. Switching Test Circuit

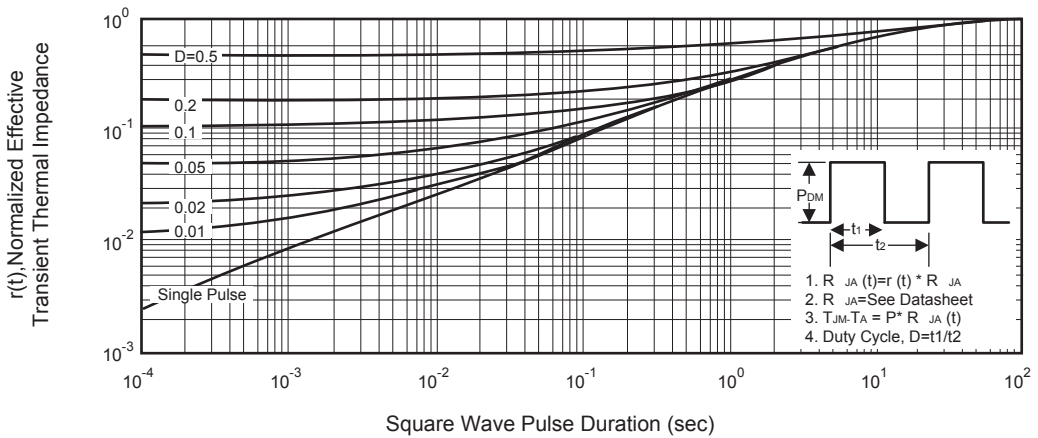


Figure 10. Normalized Thermal Transient Impedance Curve