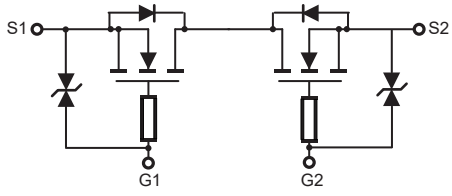
CECSP1912B

Dual N-Channel Common-Drain
Enhancement Mode Field Effect Transistor

FEATURES

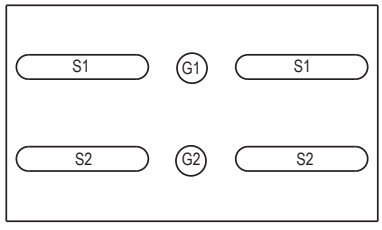


■ 12V, 19A, $R_{SS(ON)typ}$ = 2.1mΩ @V_{GS} = 4.5V.
$R_{SS(ON)typ}$ = 2.2mΩ @V_{GS} = 3.8V.
$R_{SS(ON)typ}$ = 2.4mΩ @V_{GS} = 3.1V.
$R_{SS(ON)typ}$ = 3.1mΩ @V_{GS} = 2.5V.

■ Super High dense cell design for extremely low $R_{DS(ON)}$.

■ Low gate charge operation and operation for Battery Application.

■ RoHS compliant.



3.05mm*1.77mm WLCSP

Applications

■ Portable Battery Protection.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Source-Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current-Continuous	I_S	19	A
Source Current-Pulsed [a]	I_{SM}	76	A
Maximum Power Dissipation	P_D	1.63	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	76.7	°C/W

Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Source-Source Breakdown Voltage	BV_{SSS}	V_{GS} = 0V, I_S = 1mA	12			V
Cut-Off Current	I_{SSS}	V_{SS} = 12V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 8V, V_{SS} = 0V			10	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -8V, V_{SS} = 0V			-10	μA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{SS}, I_S = 1.41mA		0.9	1.33	V
Static Source-Source On-Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 6A		2.1	2.75	mΩ
		V_{GS} = 3.8V, I_S = 6A		2.2	2.85	mΩ
		V_{GS} = 3.1V, I_S = 6A		2.4	3.95	mΩ
		V_{GS} = 2.5V, I_S = 6A		3.1	6.1	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{SS} =10V, V_{GS}= 0V, f = 1.0 KHz		6725		pF
Output Capacitance	C_{oss}			1970		pF
Reverse Transfer Capacitance	C_{rss}			1880		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 8V, I_S = 6A, V_{GS} = 4V, R_{GEN} = 3Ω		0.1		μs
Turn-On Rise Time	t_r			0.6		μs
Turn-Off Delay Time	$t_{d(off)}$			4.3		μs
Turn-Off Fall Time	t_f			17		μs
Total Gate Charge	Q_g	V_{DD} = 8V, I_S = 6A, V_{GS} = 4V		51		nC
Gate-Source Charge	Q_{gs}			7.8		nC
Gate-Drain Charge	Q_{gd}			20.8		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Voltage [c]	VF_{S-S}	V_{GS} = 0V, I_S = 6A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

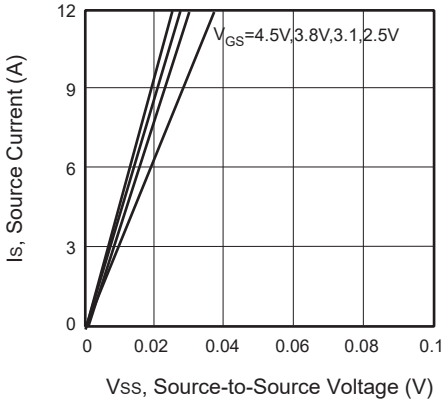


Figure 1. Output Characteristics

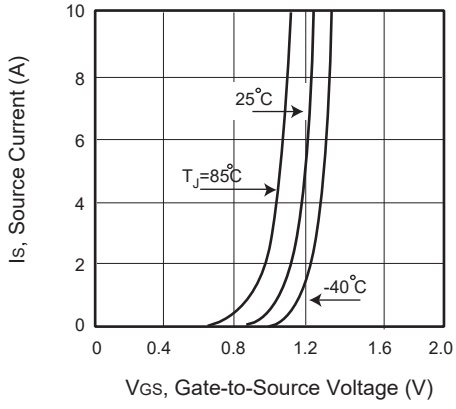


Figure 2. Transfer Characteristics

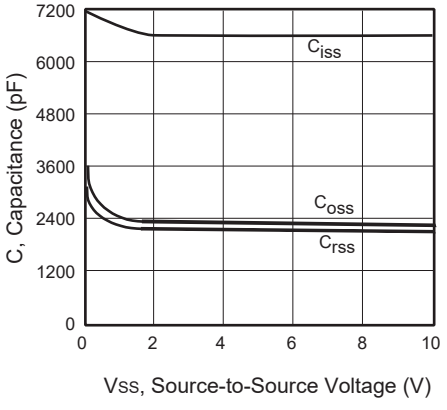


Figure 3. Capacitance

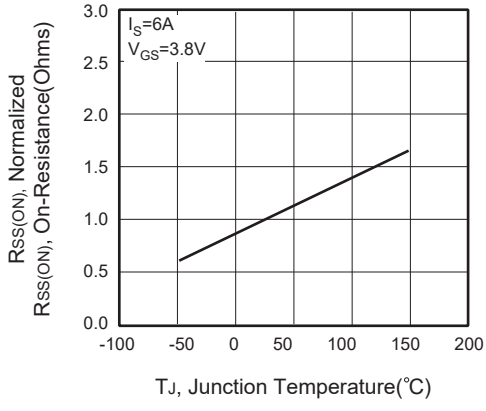


Figure 4. On-Resistance Variation with Temperature

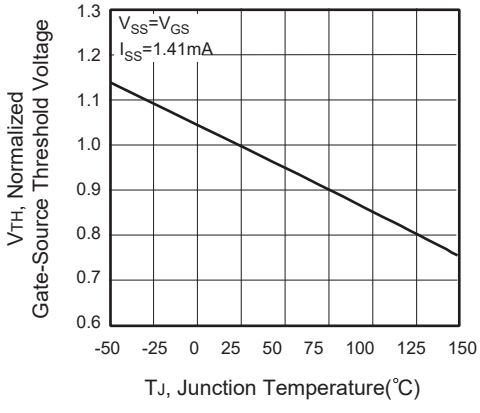


Figure 5. Gate Threshold Variation with Temperature

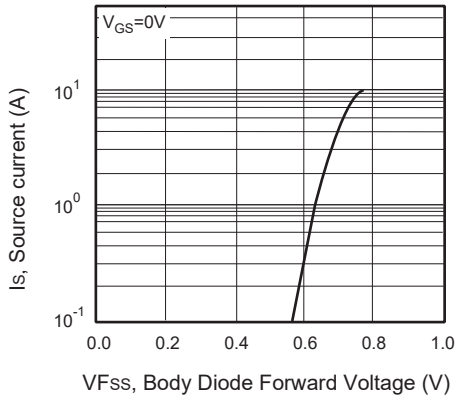


Figure 6. Body Diode Forward Voltage Variation with Source Current

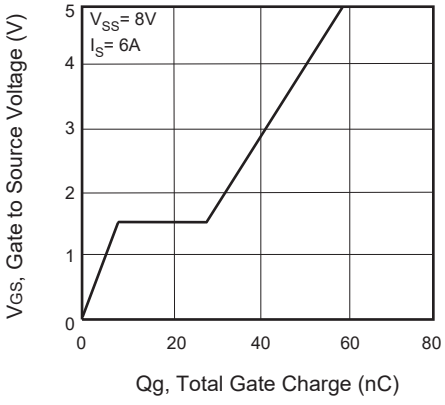


Figure 7. Gate Charge

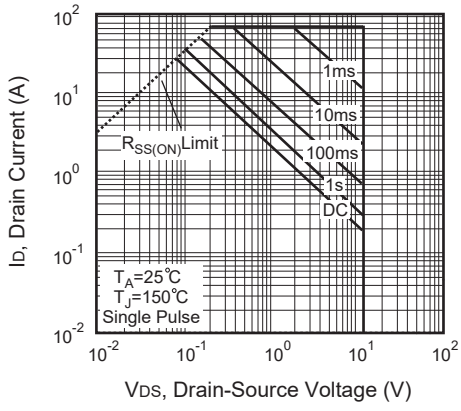


Figure 8. Maximum Safe Operating Area

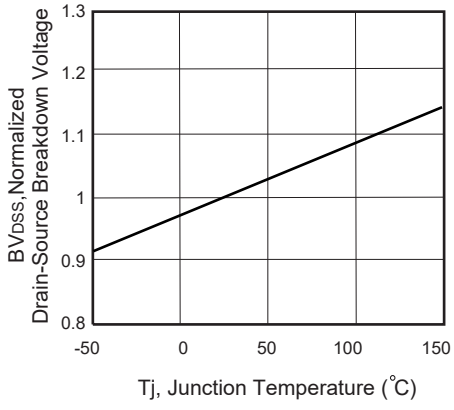


Figure 9. Breakdown Voltage Variation VS Temperature

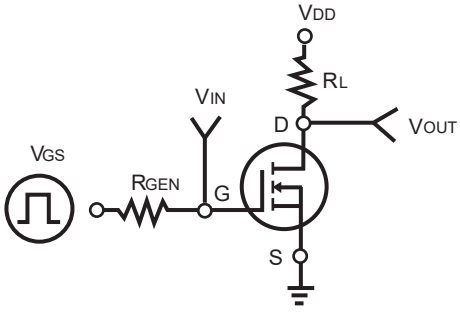


Figure 10. Switching Test Circuit

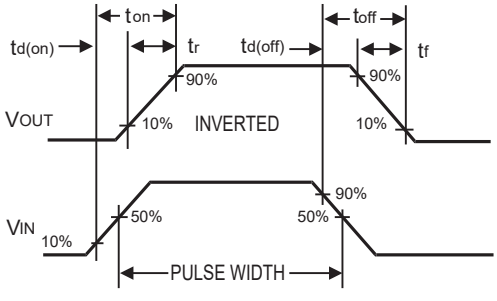


Figure 11. Switching Waveforms

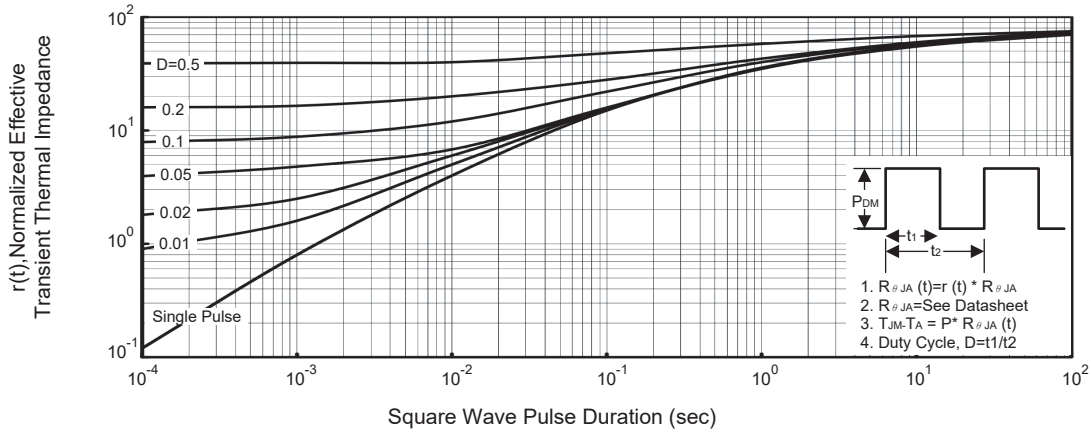
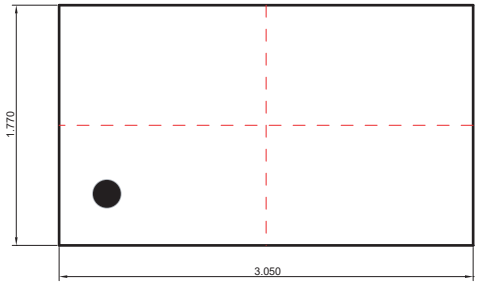
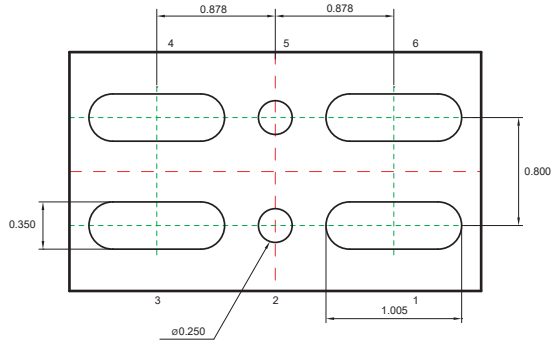


Figure 12. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE





Standard Tolerance: ±0.03mm